



PCB 1G7 LA-D822P REV0 M/B UMA
DA80017E000

Compal Confidential

Dali & Astro BKA40/BKA50/BKD40/BKD50 MB Schematic Document

LA-D822P
Rev: 1.0 (A00)
2016.06.06

UC1 KBL_15W_B@



SA0000A382L
KBL U SR2VN
S IC FJ8067702739738 SR2VN H0 2.4G A31!

UC1 KBL_15W_I5@



SA0000A372L
KBL U SR2VL
S IC FJ8067702739739 SR2VL H0 2.5G A31!

UC1 KBL_15W_I7@



SA0000A342L
KBL U SR2VM
S IC FJ8067702739740 SR2VM H0 2.7G A31!

UC1 KBL_15W_2+1@



SA00009QM0L
KBL U QKKQ
S IC A31 FJ8067702739920 QKKQ G0 1.7G

UC1



UC1 SKL_15W@



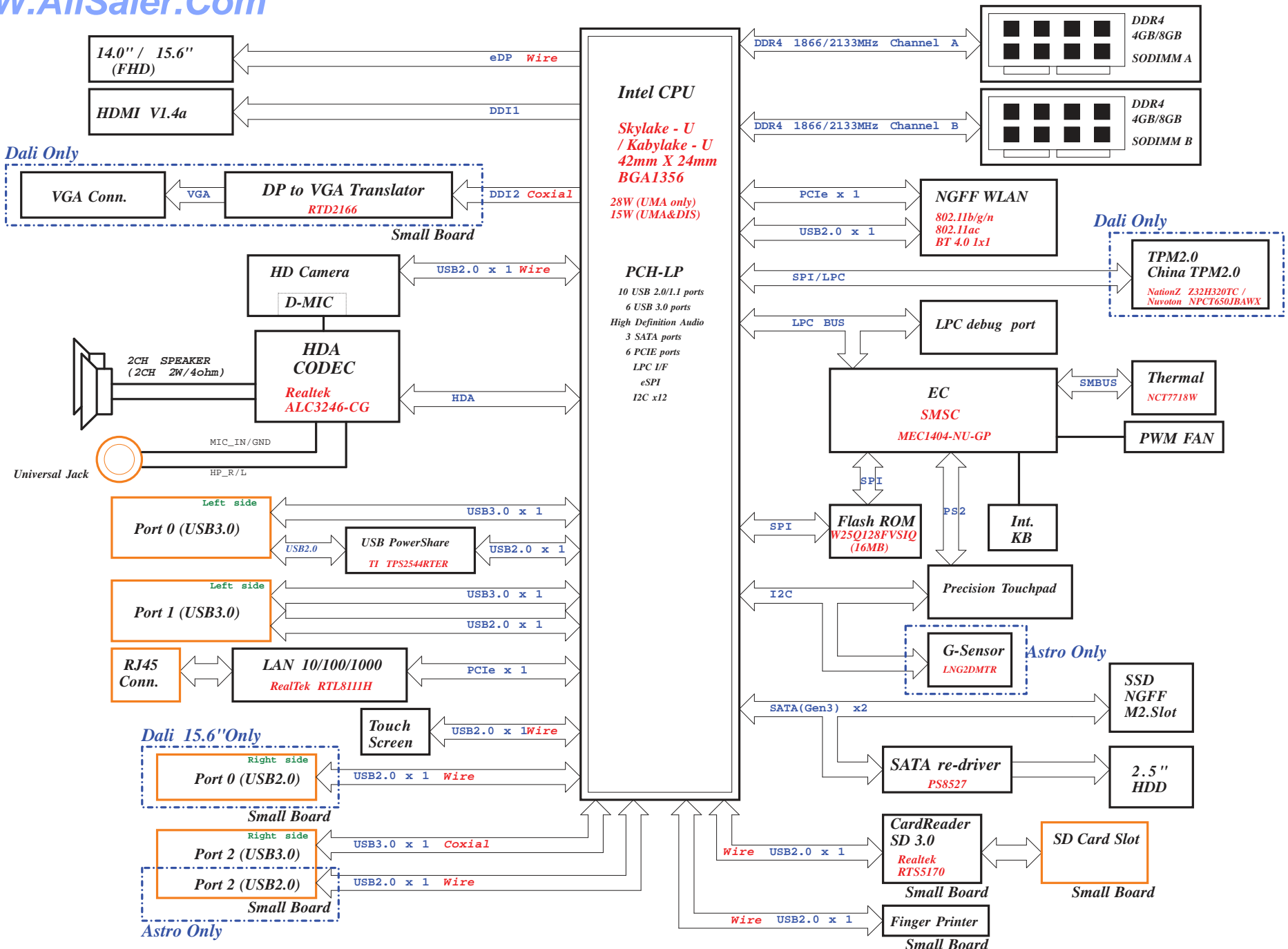
SA000092N4L
SKL U I3-6100U
S IC FJ8066201931104 SR2EU D1 2.3G A31!

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PM TABLE

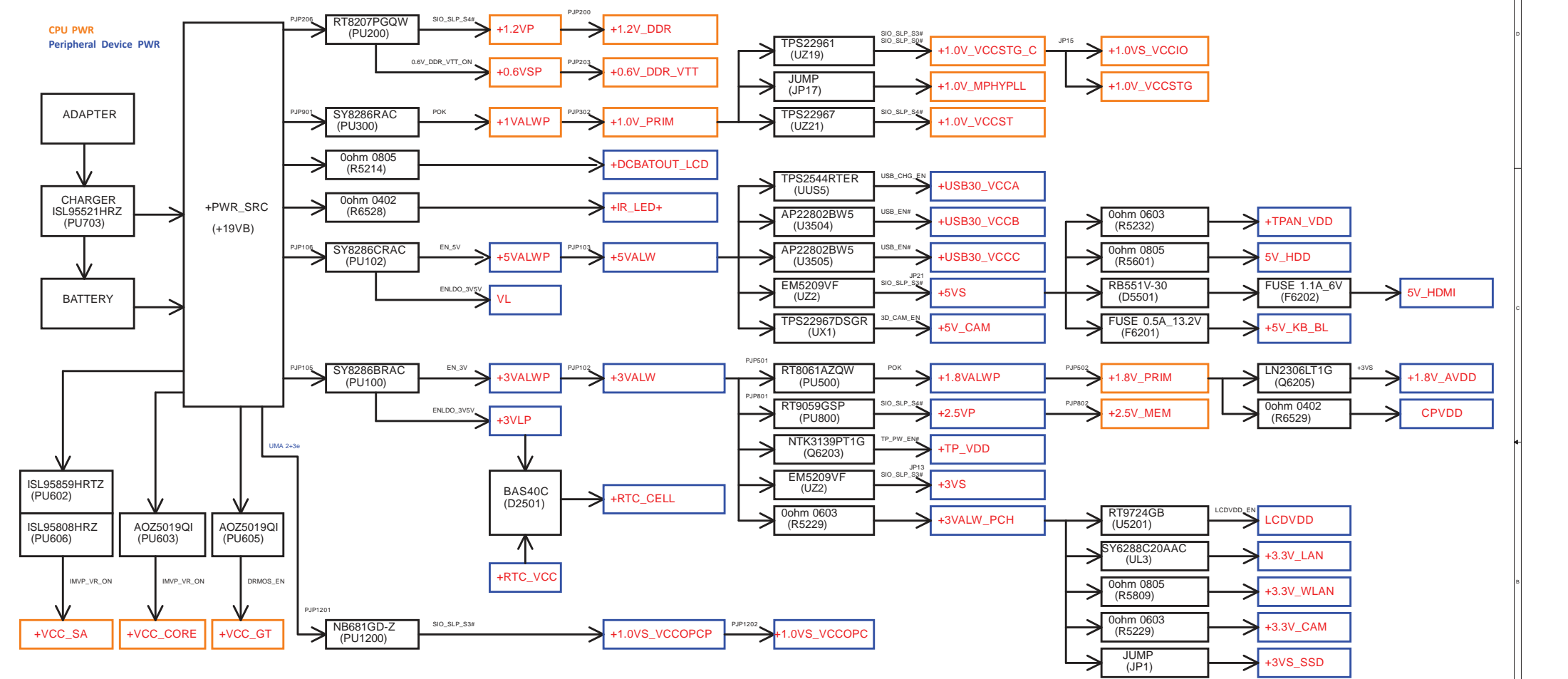
power plane State	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +1.8VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	DVT1(X01)
3	100	17.8	2.801	DVT2(X02)
4	100	22.1	2.703	Pilot(A00)
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	Touch Screen
8	BT
9	Finger Printer
10	N/A

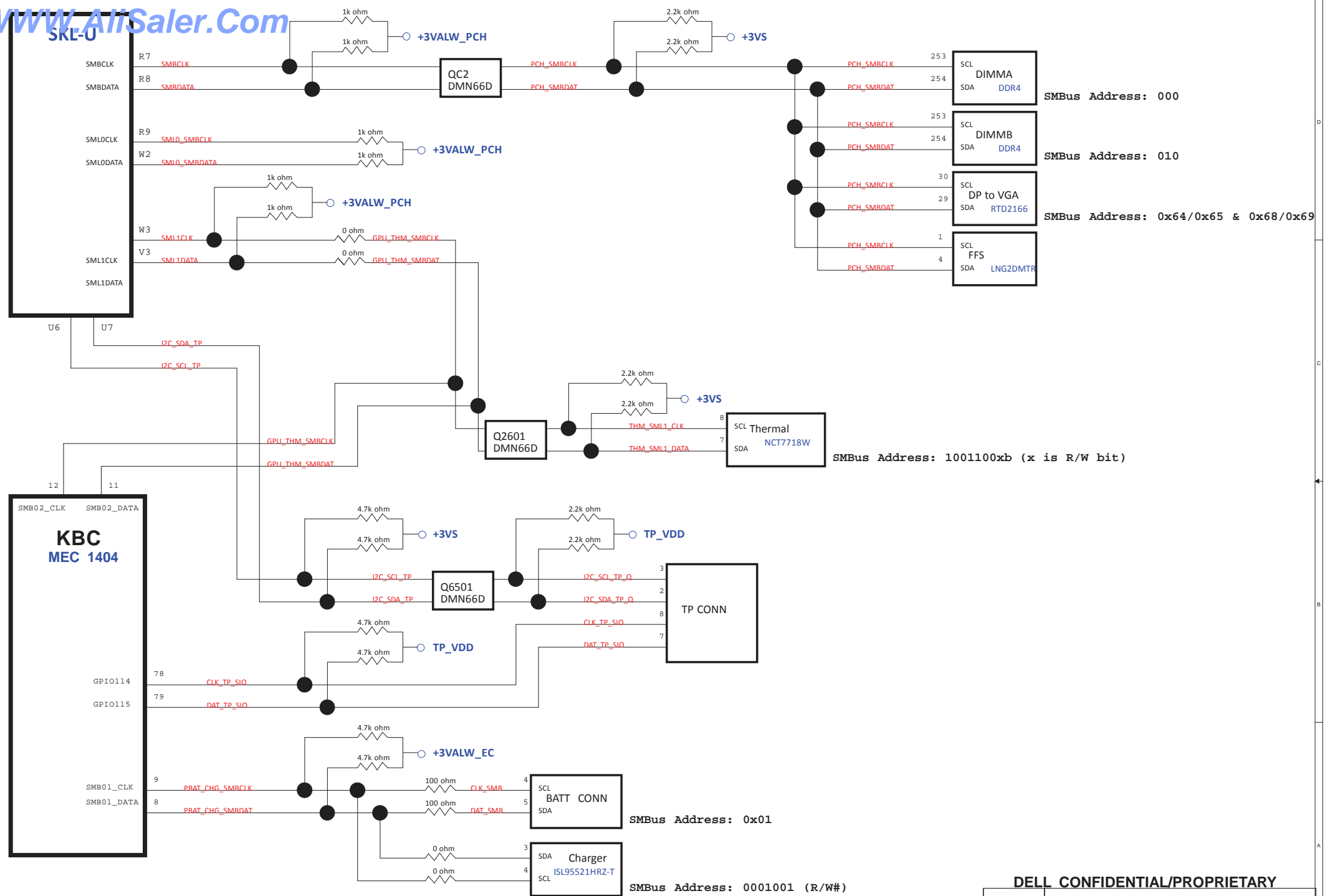
USB3.0	SSIC	PCIE	SATA	DESTINATION
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USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		N/A
USB3.0-6		PCIE-2		N/A
		PCIE-3		N/A
		PCIE-4		N/A
		PCIE-5		WLAN
		PCIE-6		GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	SATA SSD




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Power Rail			
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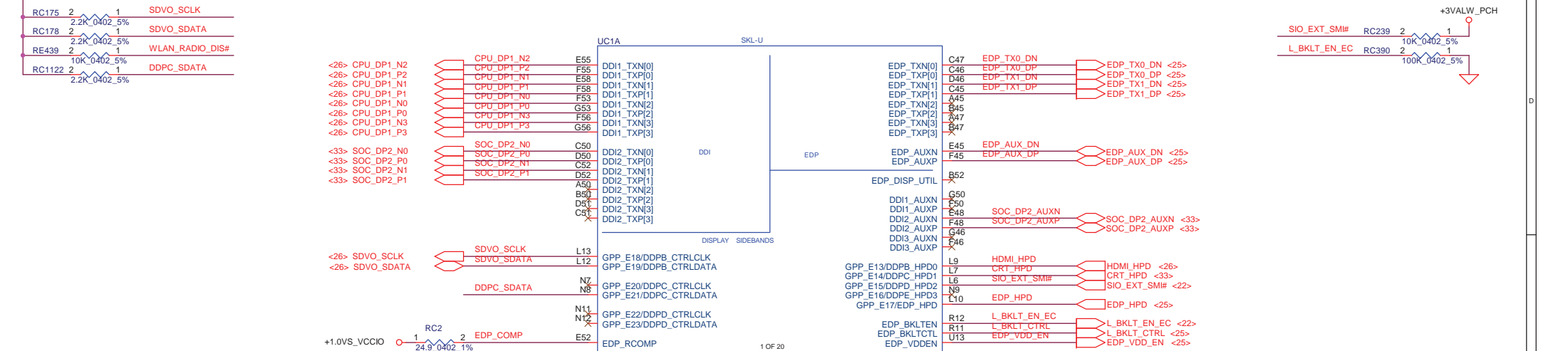
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SMBus Block Diagram

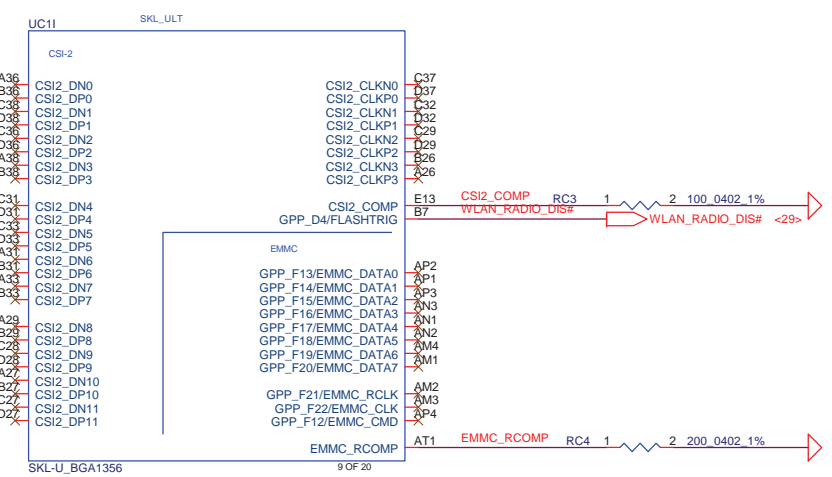
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SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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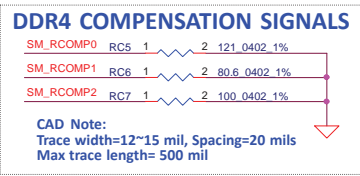
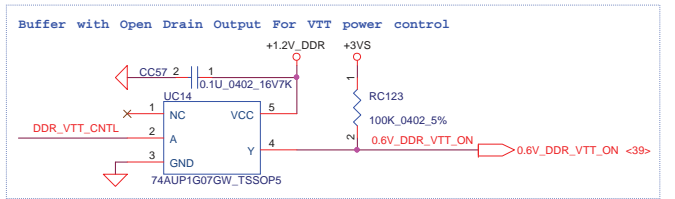
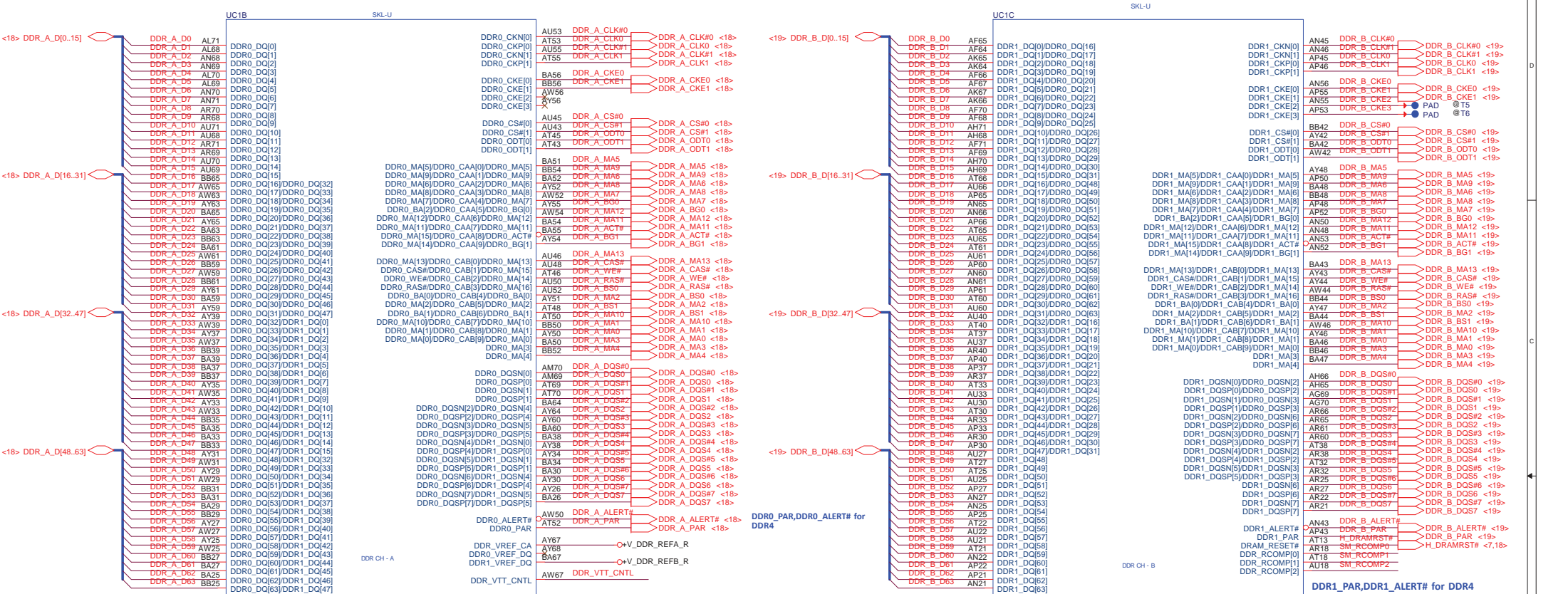
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MCP(1/14)DDI,EDP,CSI2,EMMC

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MCP(2/14)DDR4

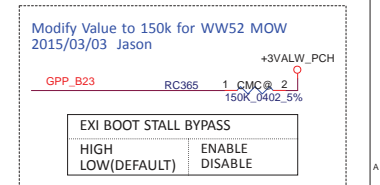
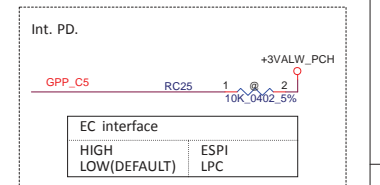
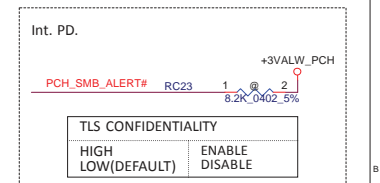
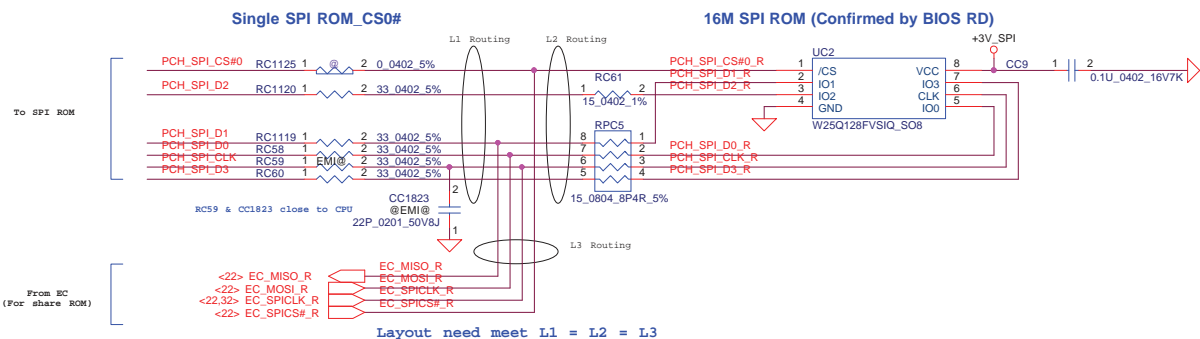
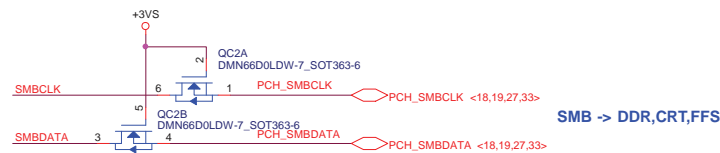
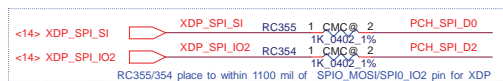
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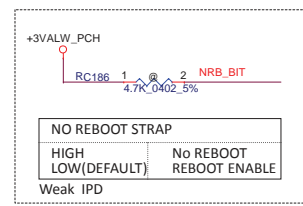
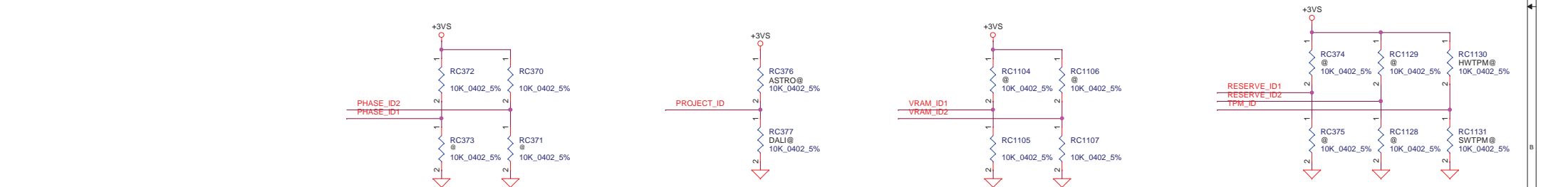
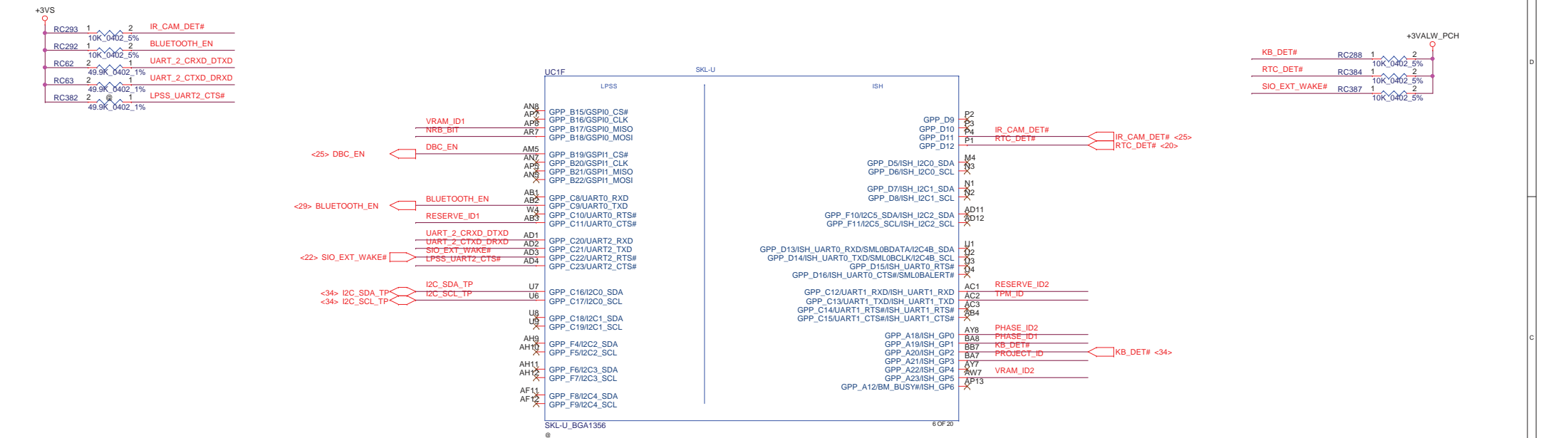
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PHASE ID	PHASE ID1 (GPP_A19)	PHASE ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1

PROJECT ID	PROJECT ID (GPP_A21)
Dali	0
Astro	1

VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2 (GPP_A23)	VRAM_ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
Reserved	1	1

PROJECT ID	TPM_ID (GPP_C13)
SW_TPM	0
HW_TPM	1

RESERVE ID	RESERVE_ID1 (GPP_C11)	RESERVE_ID2 (GPP_C12)

Win7 Debug solution

Option 2 : For Open Chassis Platforms

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MCP(4/14)GSPi,I2C,UART,ISH

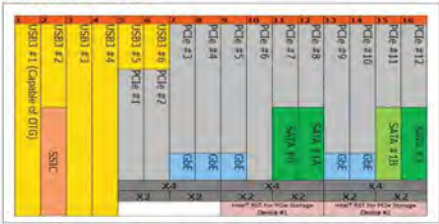
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Figure 3-3 Hsio Mapping on SKL PCH U



- There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:
- Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
 - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
 - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as x4, x2, 1x2 + x4, or 1x4.
 - Up to 3 SATA ports (multiplexed with PCIe*)
 - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
 - Up to 6 USB 3.0 ports (multiplexed with PCIe*)
 - USB Dual Role (OTG) capability is available on USB 3.0 Port 1.
 - One SSIC x1 port is multiplexed with USB 3.0 Port 2.
 - One GbE line:
 - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10.
 - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
 - Up to 2 Intel RST for PCIe* storage devices supported
 - Devices can be x2 or x4.
 - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12.

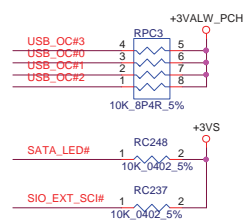
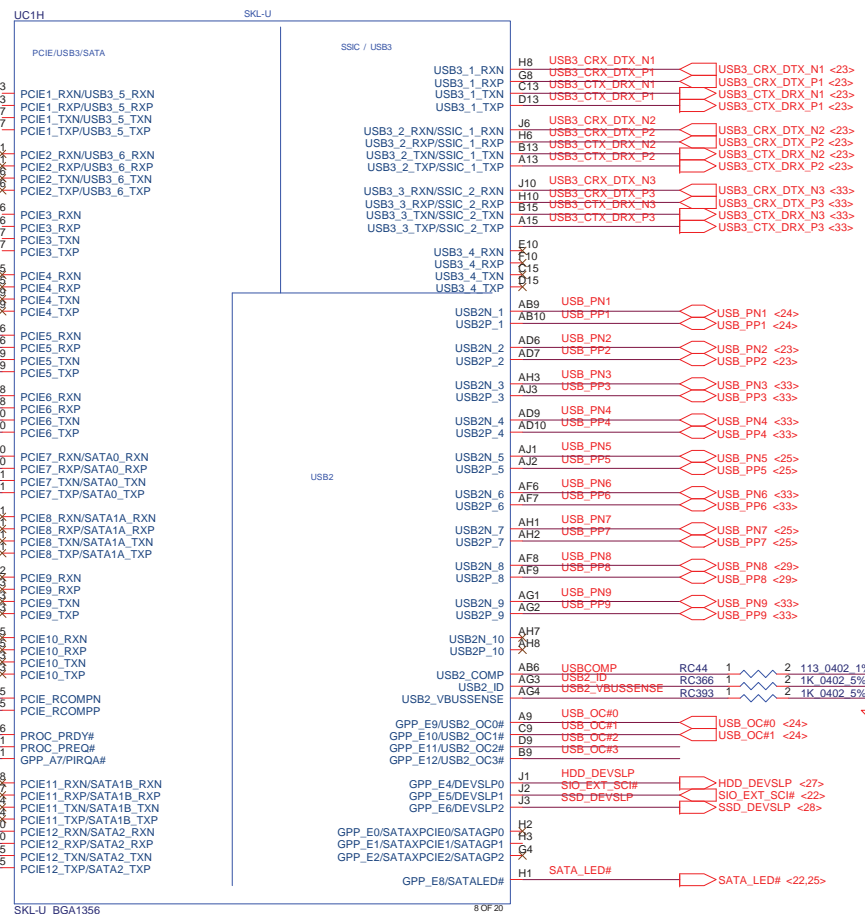
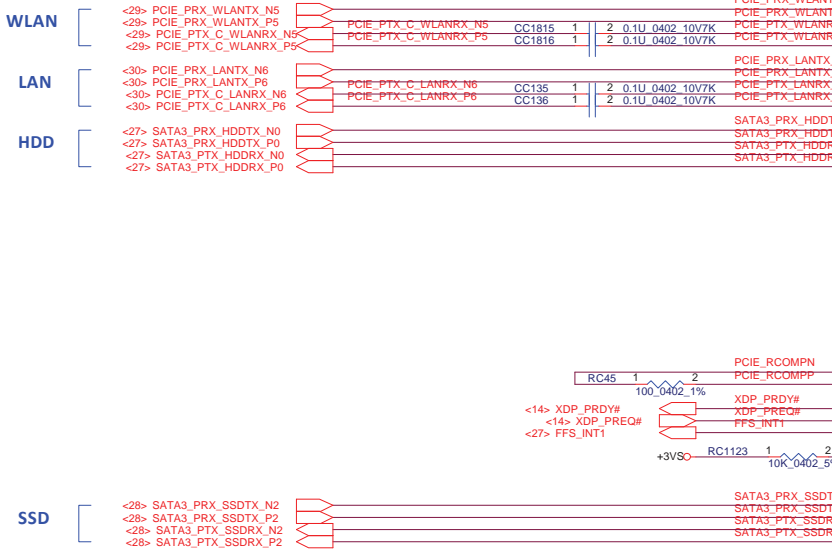


Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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MCP(5/14)PCIE,USB,SATA

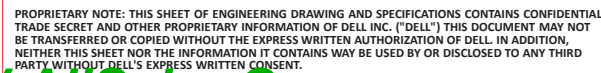
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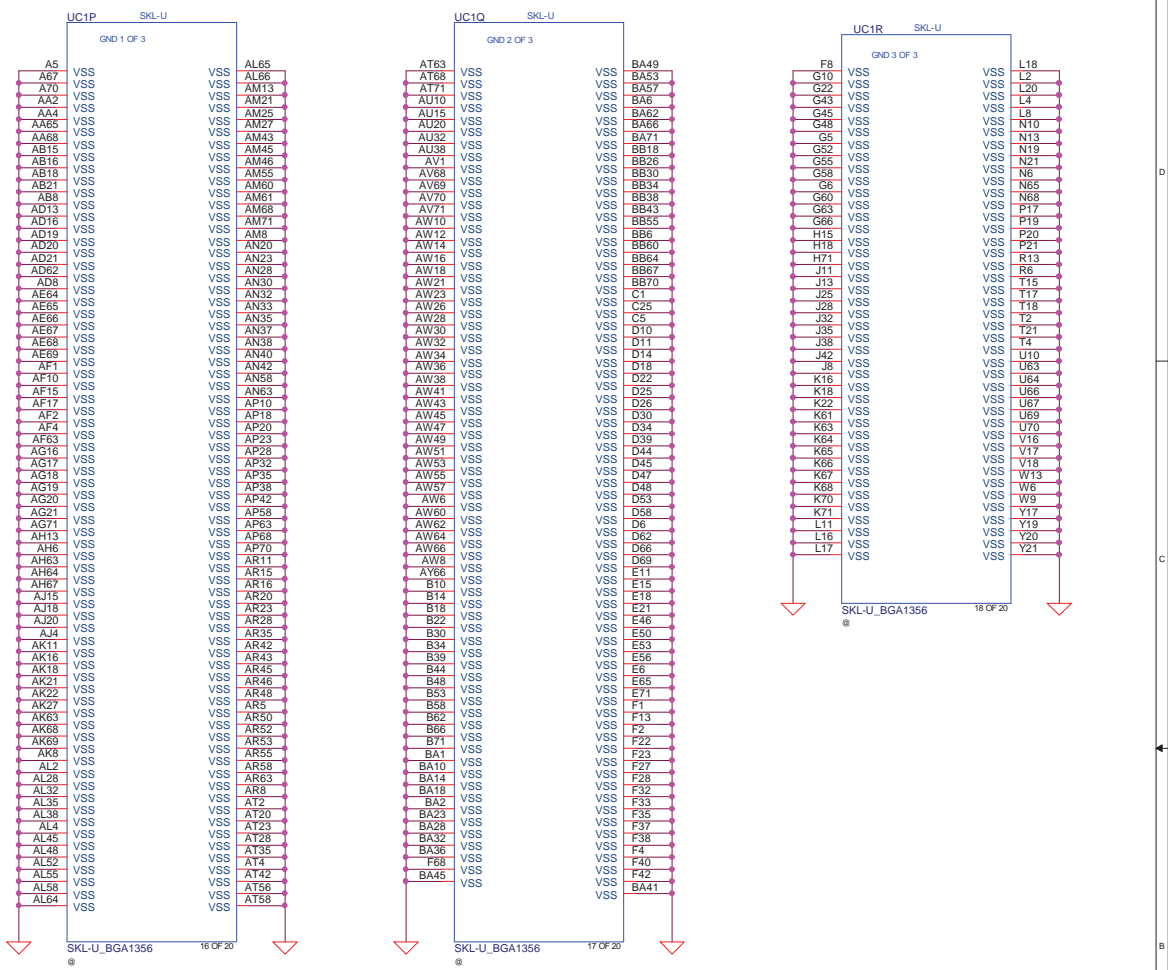
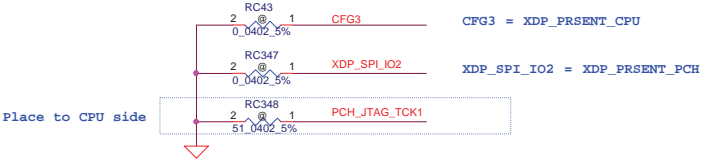
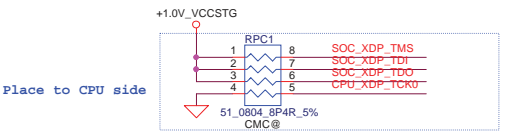
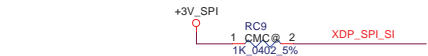
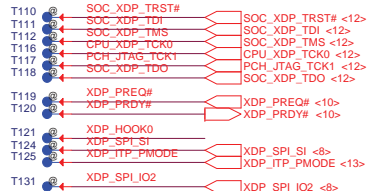
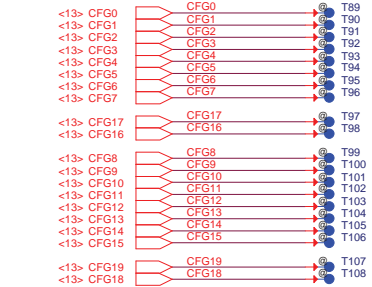
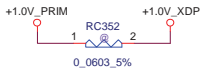
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PRIMARY CMC CONN



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

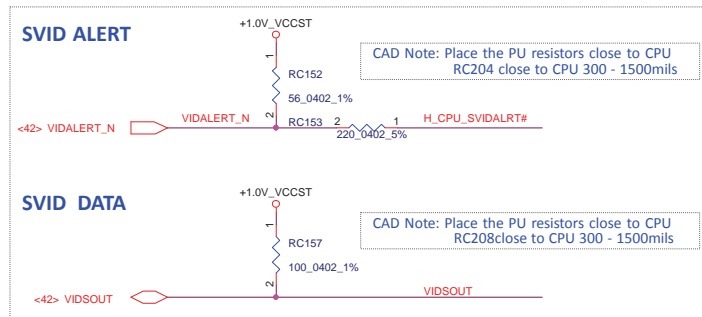
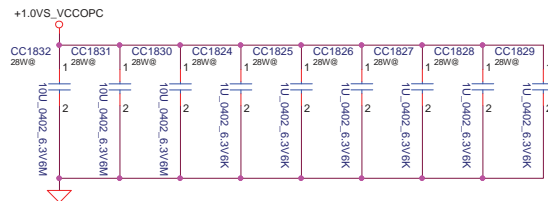
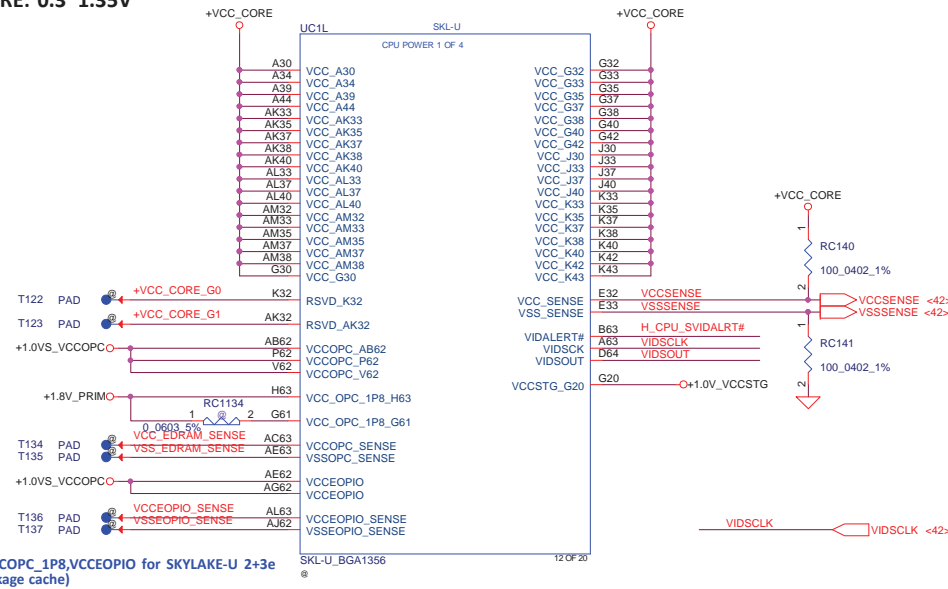
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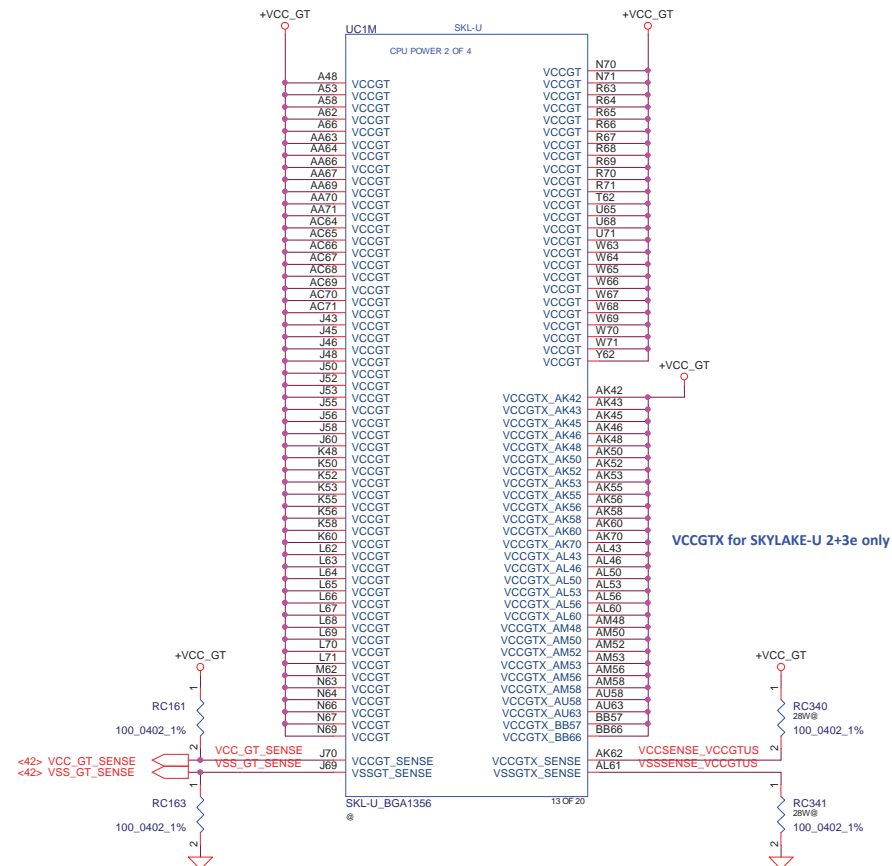
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Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.3~1.35V



+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

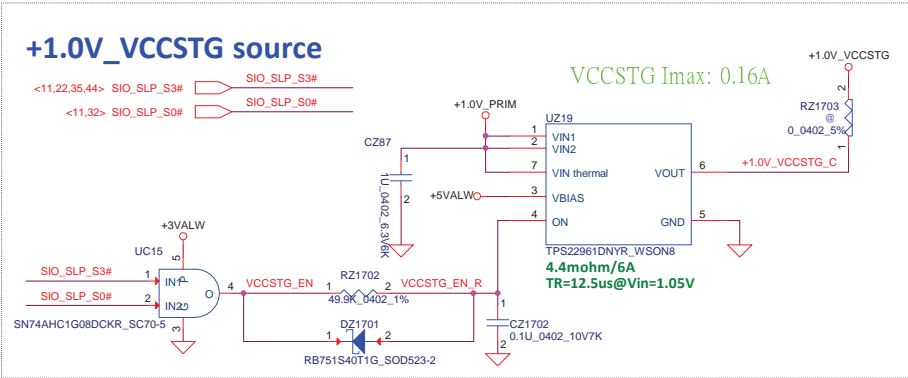
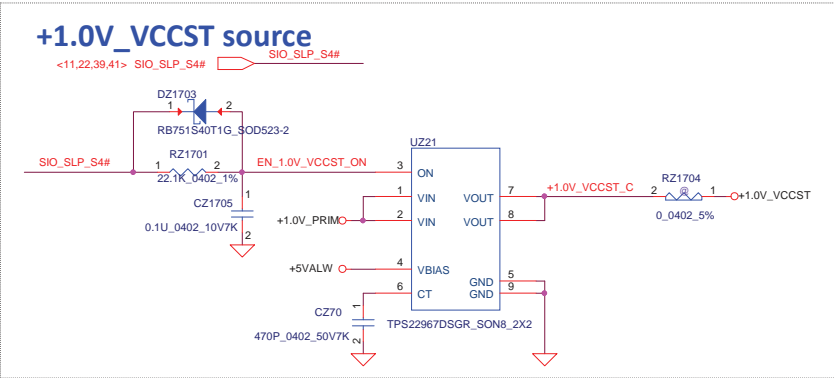
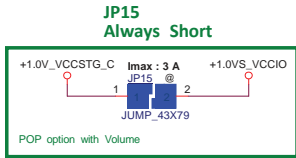
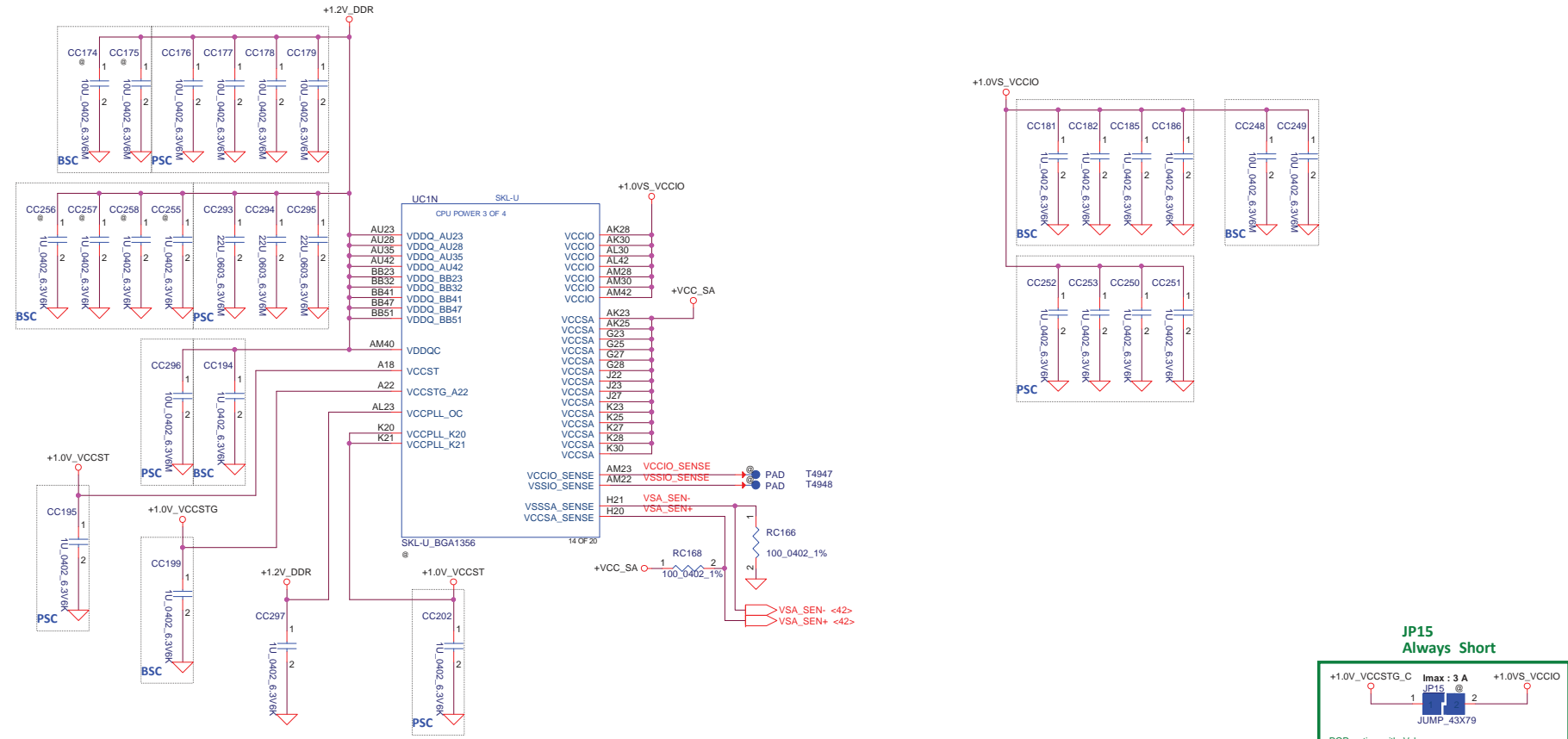


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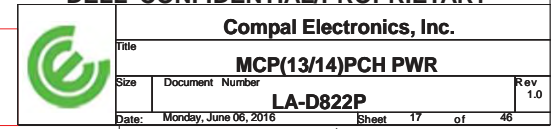
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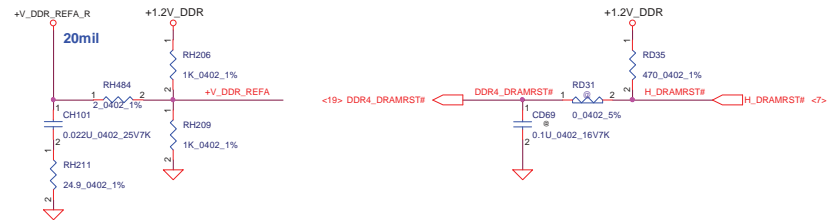
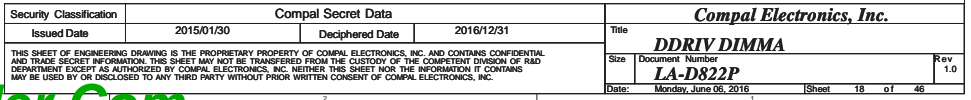


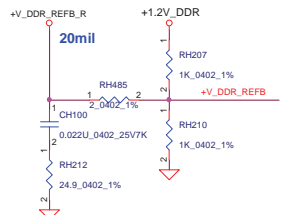
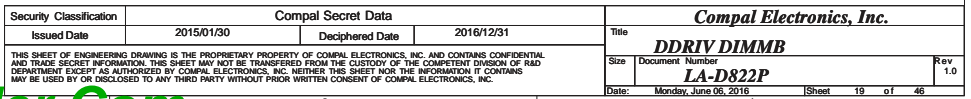
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Compal Electronics, Inc.				
MCP(12/14)PWR-VCCIO, MEM				
LA-D822P				
Rev 1.0				
Size	Document Number	Date: Monday, June 06, 2016		
Sheet	16	of	46	

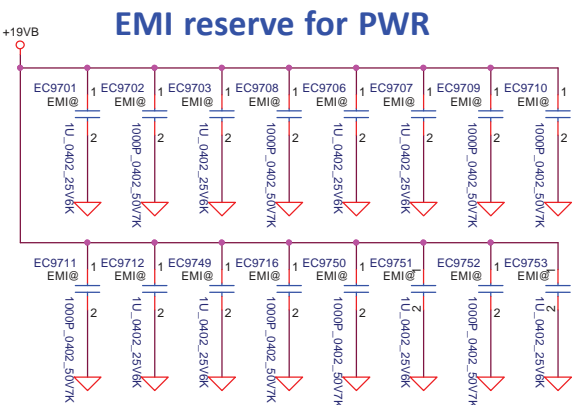
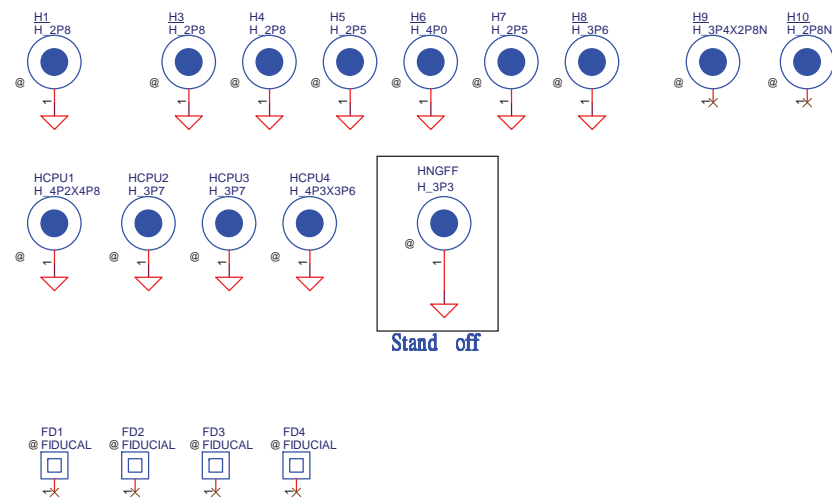


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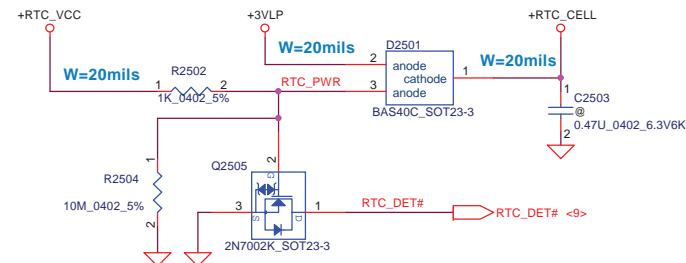




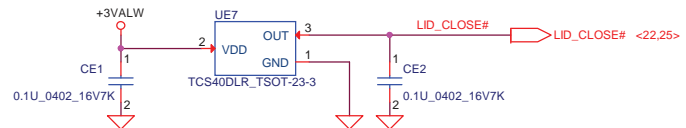
Screw hole/FD/EMI stop



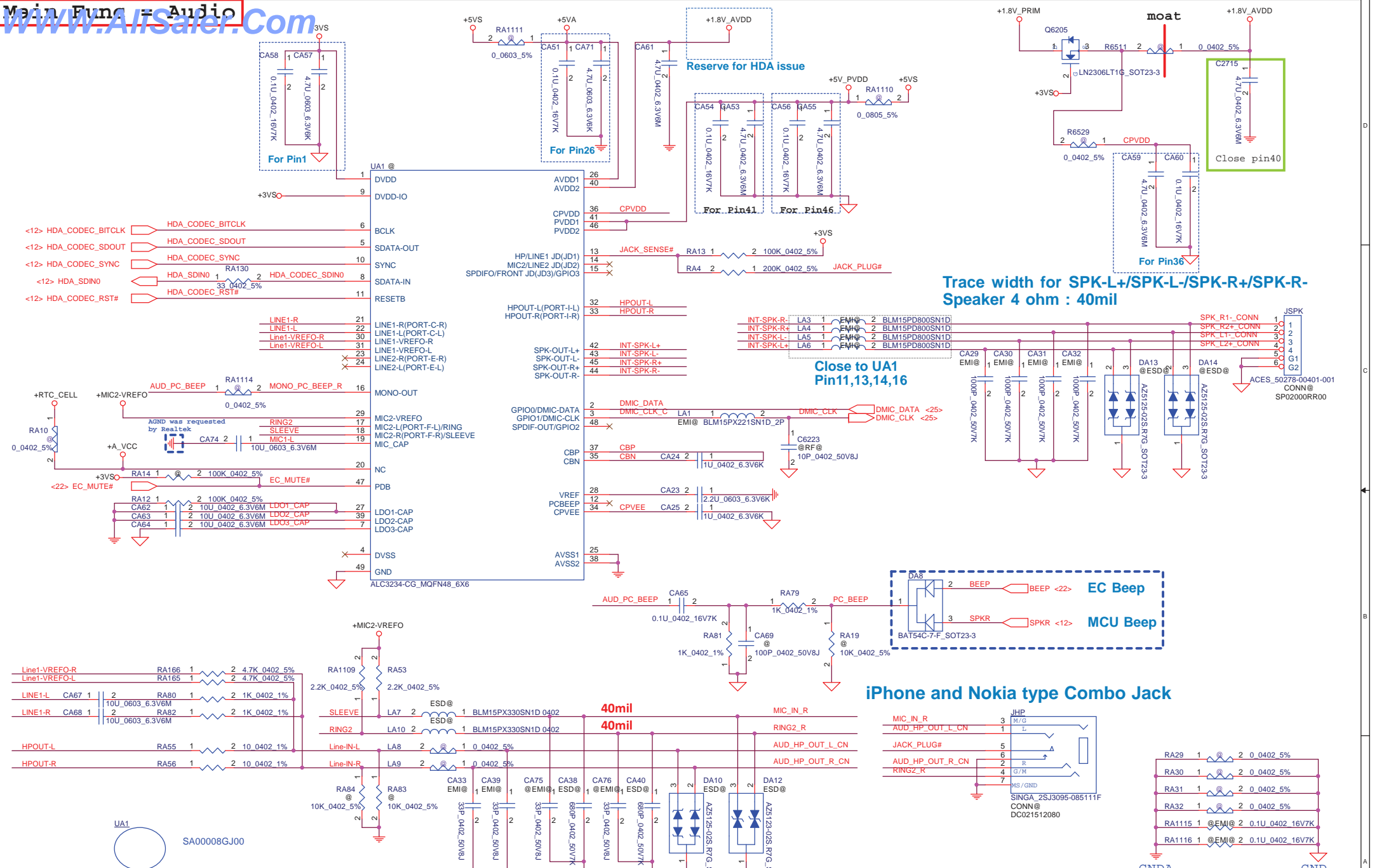
Main Func = RTC



Main Func = LID Switch



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Size	Document Number	Rev		1.0	
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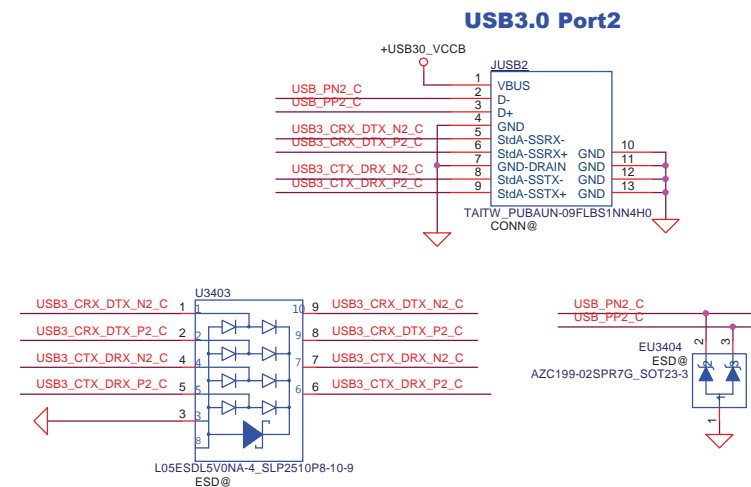
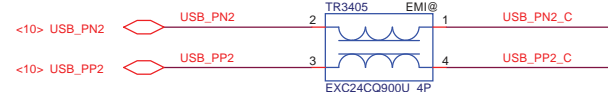


Diff Table

IC \ PIN	PIN4	PIN11	PIN12	PIN16	PIN20	PIN36
ALC3234	DVSS	RESETB	PCBEEP	MONO-OUT	NC	CPVDD(3.3V)
ALC3246	DC_DET	I2C_SDA	I2C_SCL	PCBEEP	5VSTB	CPVDD(1.8V)

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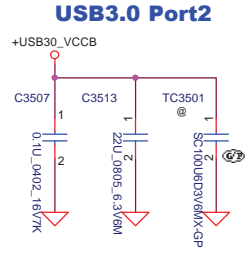
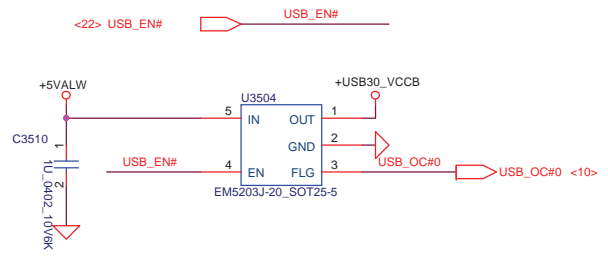
Compal Electronics, Inc.			
Title			
Audio Codec ALC3246			
Size	Document Number		Rev 1.0
LA-D822P			
Date:	Monday, June 06, 2016	Sheet 21 of 46	



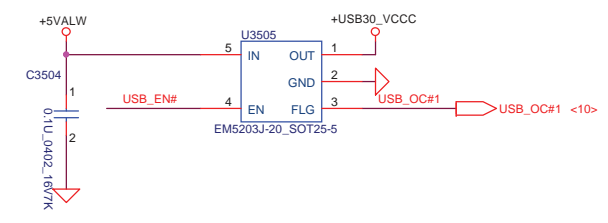
WWW.AliSaler.Com

Main Func = USB3.0 Port2

WWW.AliSaler.Com

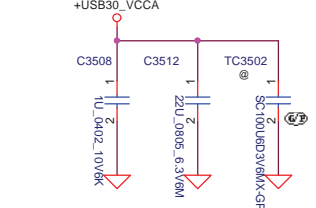
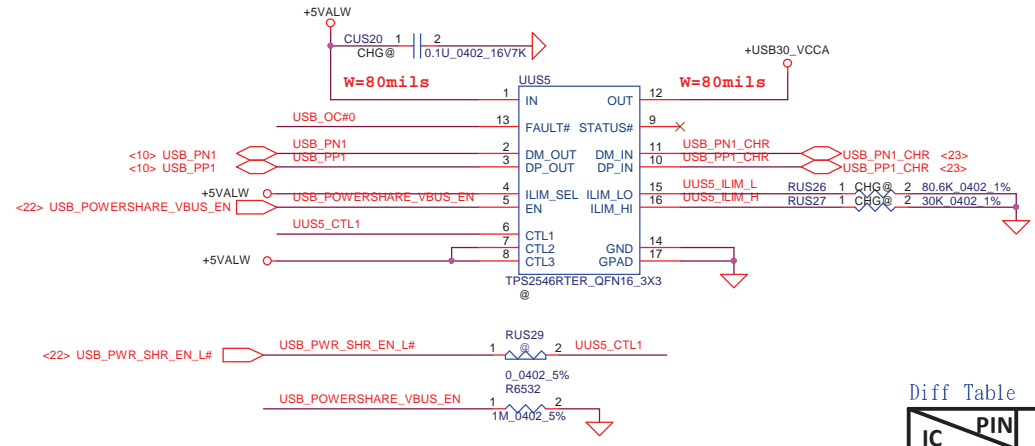


Main Func = USB3.0 Port3 / USB2.0 Port



USB3 Port3/USB2 Port1 (IO Board)

Main Func = USB Chager



Charger CT
EC GPIO
S0/S3 (CDP)
S4/S5 (DCP)

CTL1
GPIOA07(pin104)
1
0

CTL2
GPIO22(pin41)
1
1

CTL3
GPIOA11(pin108)
1
1

ILIM_SEL
GPIO21(pin40)
1
1

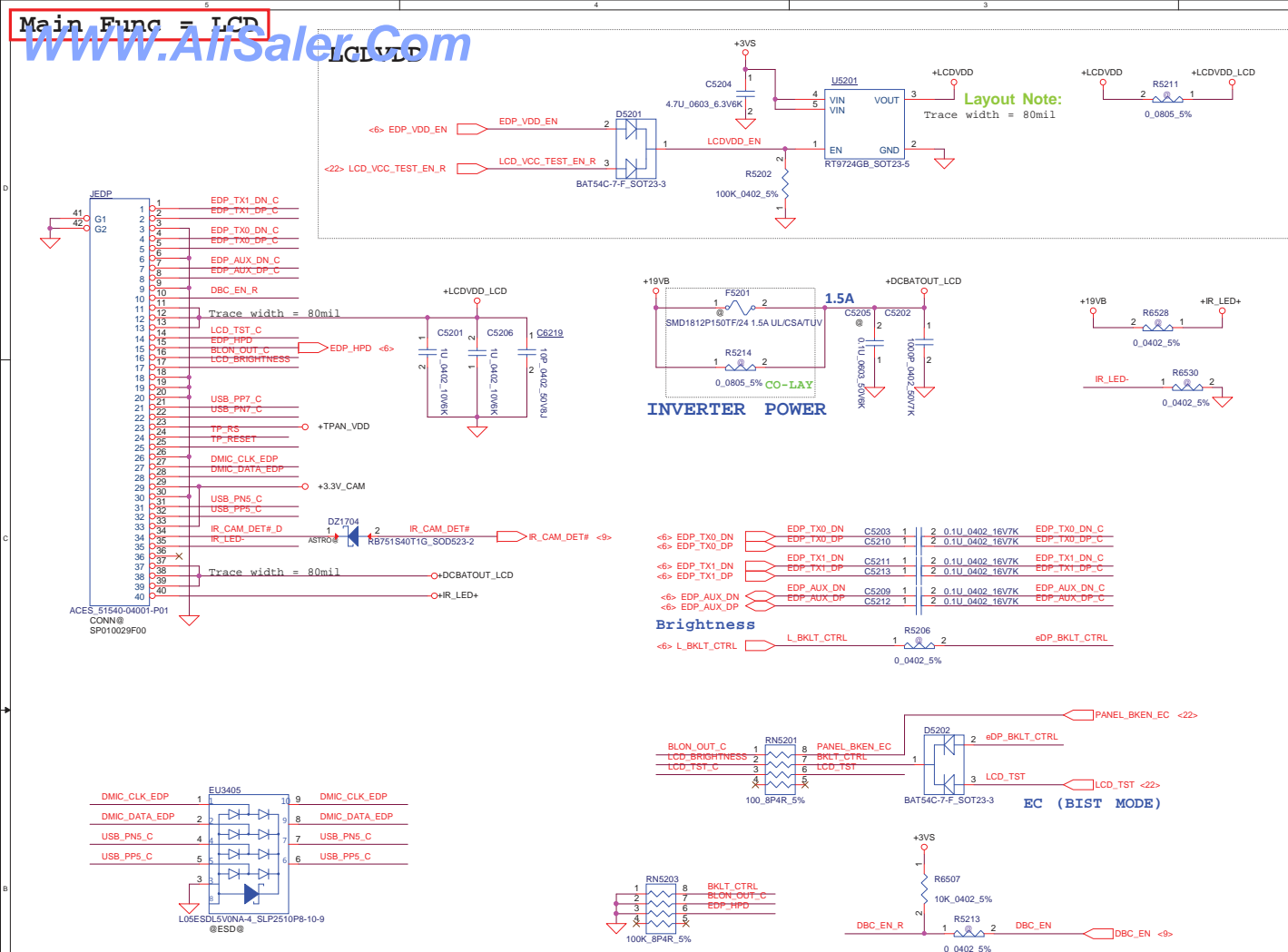
Diff Table

IC	PIN	PIN9
TPS2546	STATUS#	
TPS2544	NC	

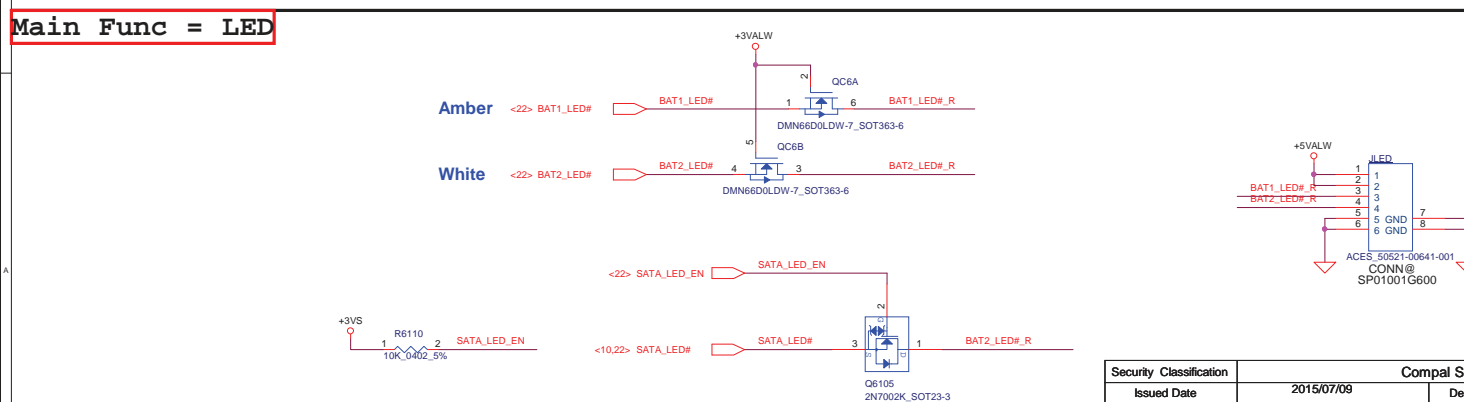


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				Document Number	
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				1.0	
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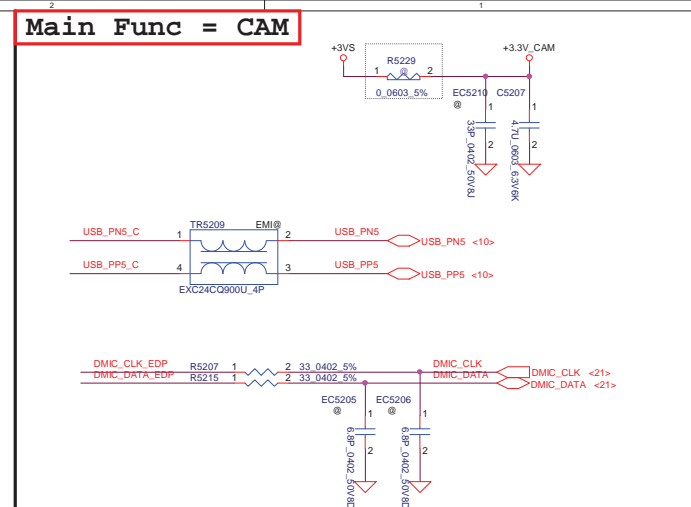
5
Main Func = LCD



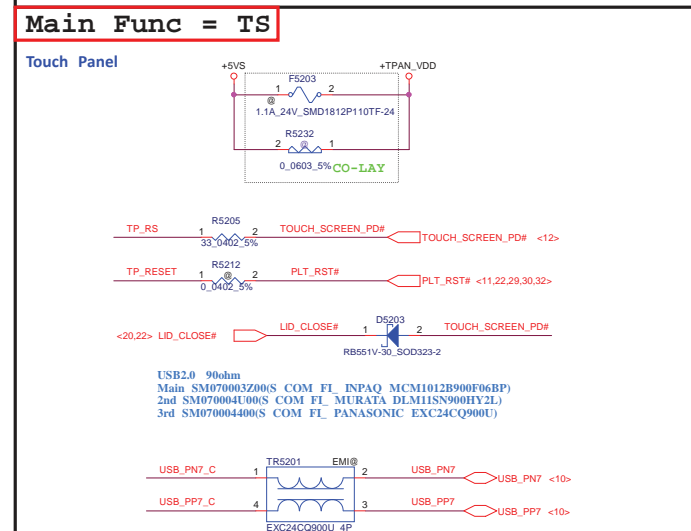
```
Main Func = LED
```



2	
Main Func = CAM	

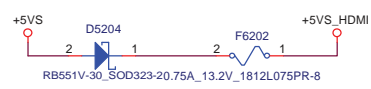


Main Func = TS

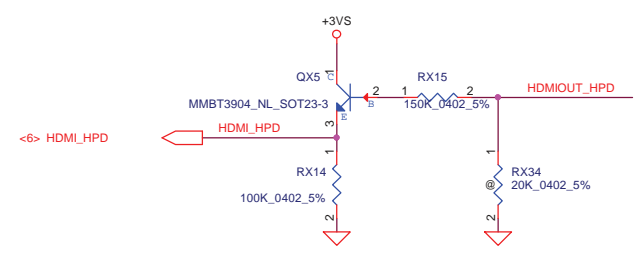
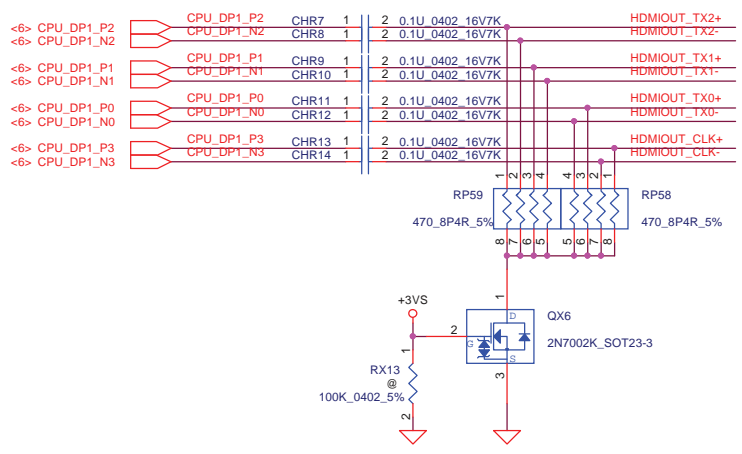
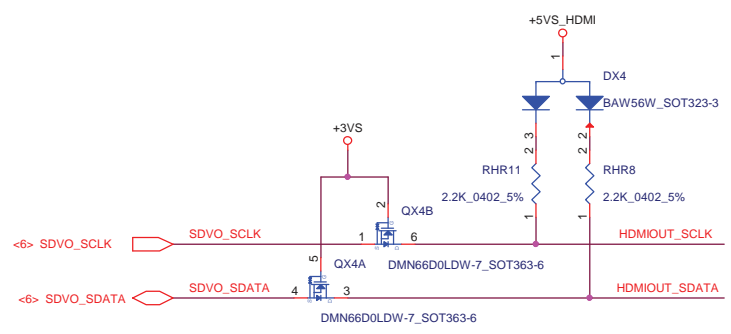
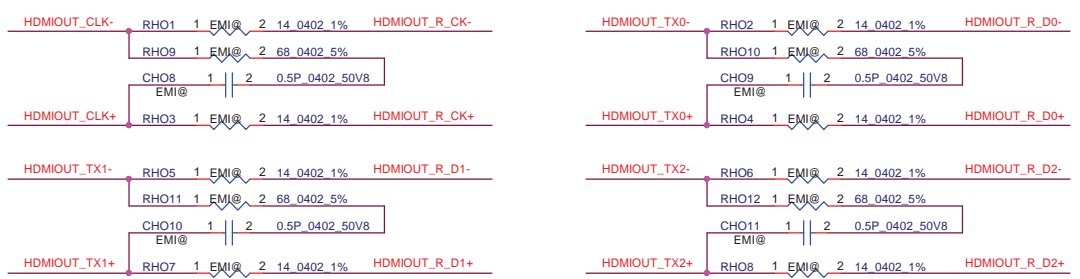
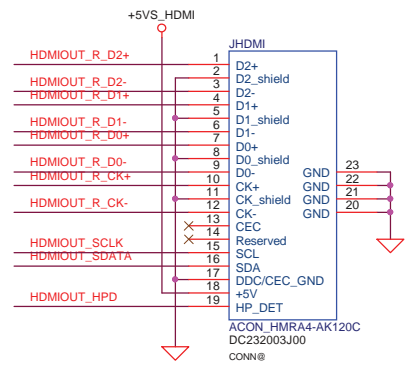


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Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	
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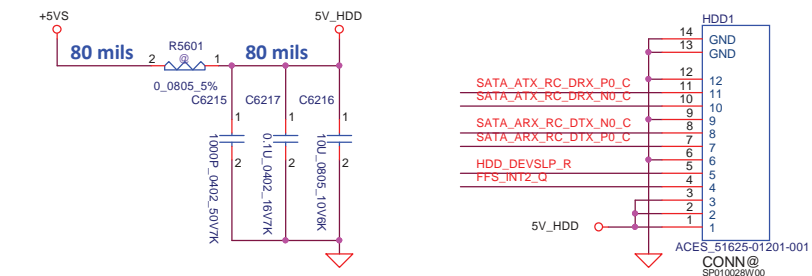
2014.12.25
1. LHO1, LHO2, LHO3, LHO4 change root pin (SI ZE : 050 4) and unpp
2. RHO1, RHO3, RHO5, RHO7, RHO2, RHO4, RHO6, RHO8, RHO13, RHO14, RHO15, RHO16, change to pop.





HDMI-OUT Connector



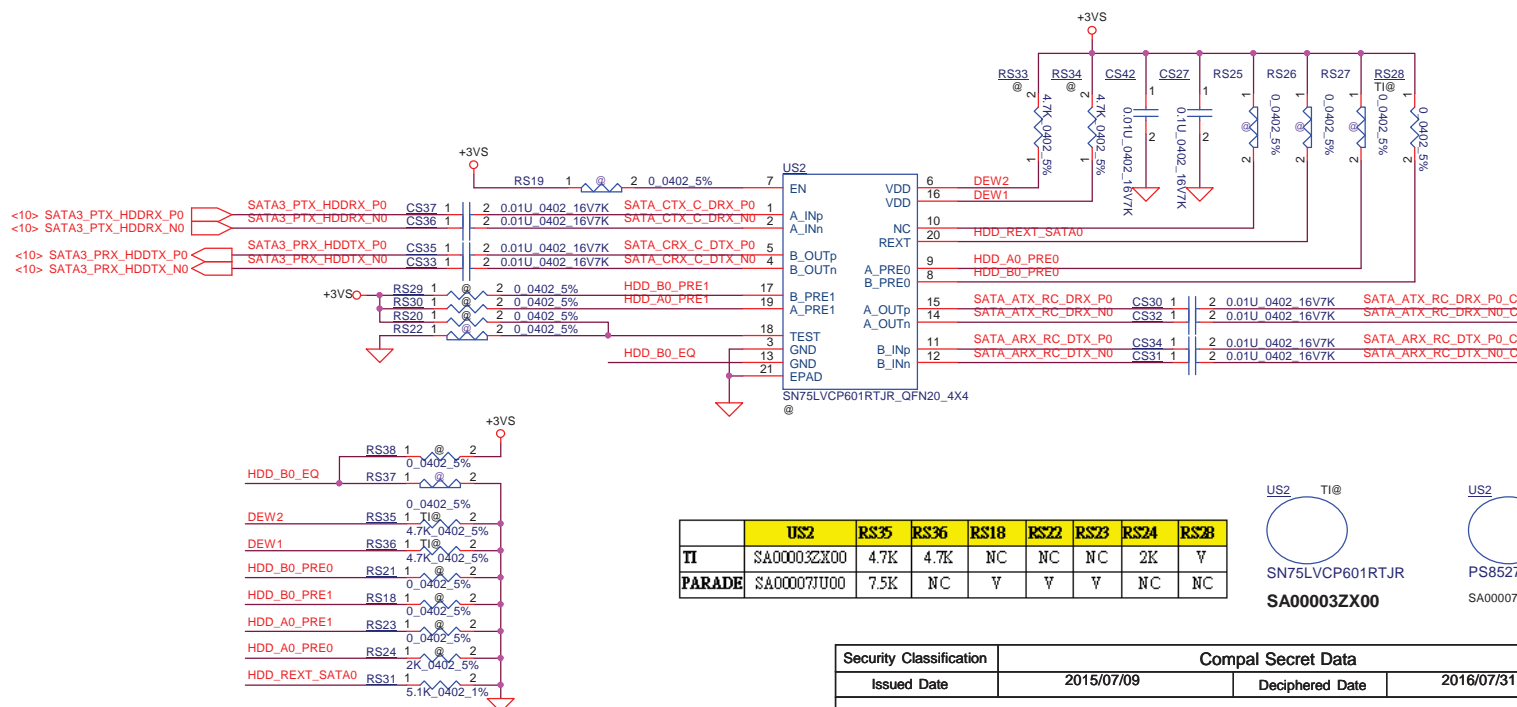
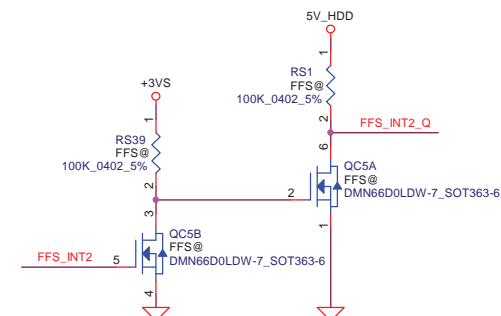
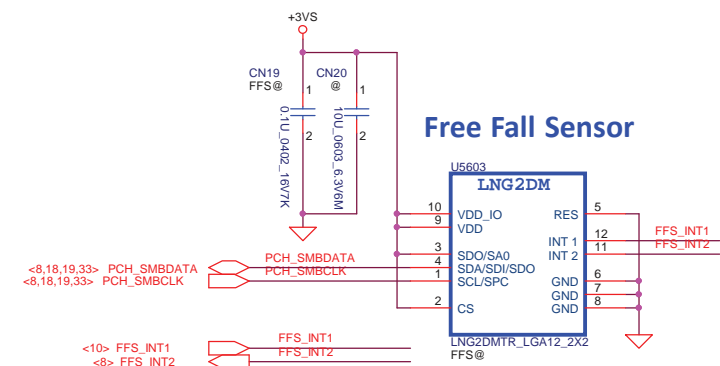
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<10> HDD_DEVSPLP  HDD_DEVSPLP R5605 2  1 0.0402 5% HDD_DEVSPLP_R

Reserve, refer to M15 EE Implementation Requirements

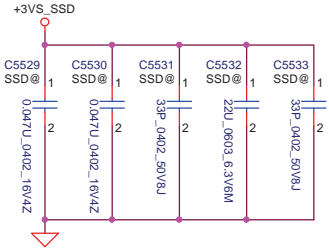
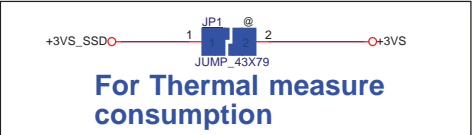
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	



	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS25
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007U00	7.5K	NC	V	V	V	NC	NC

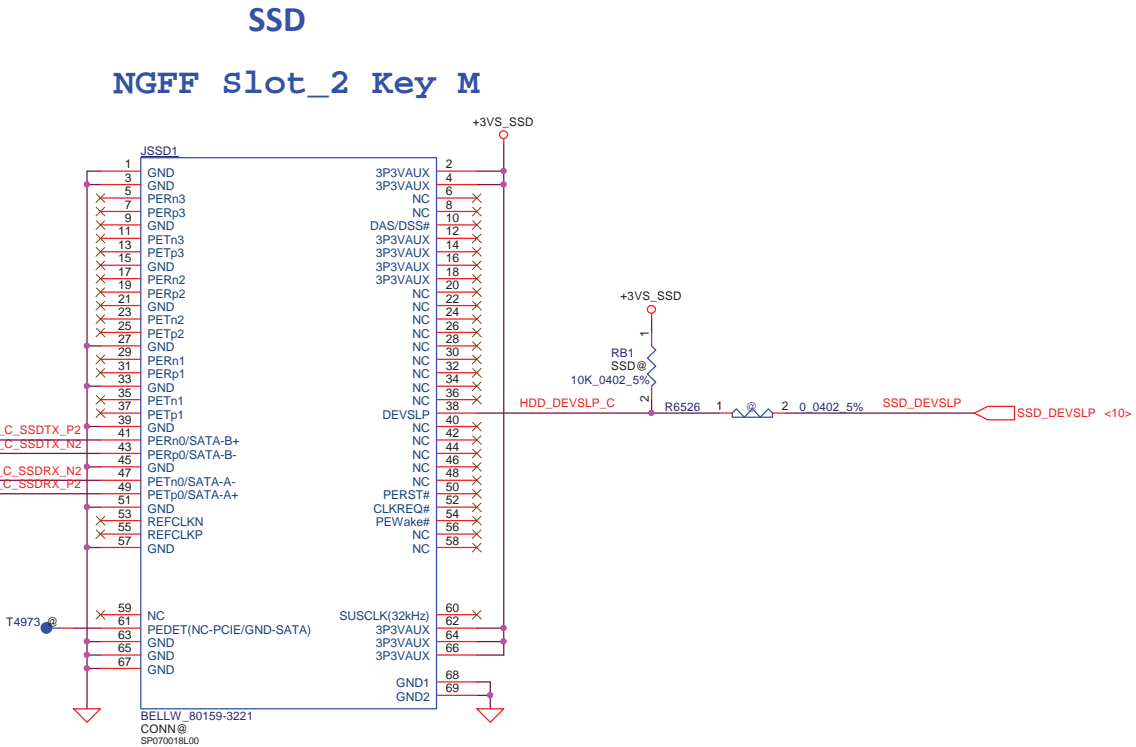


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				HDD+Sensor				
				Size	Document Number		Rev	
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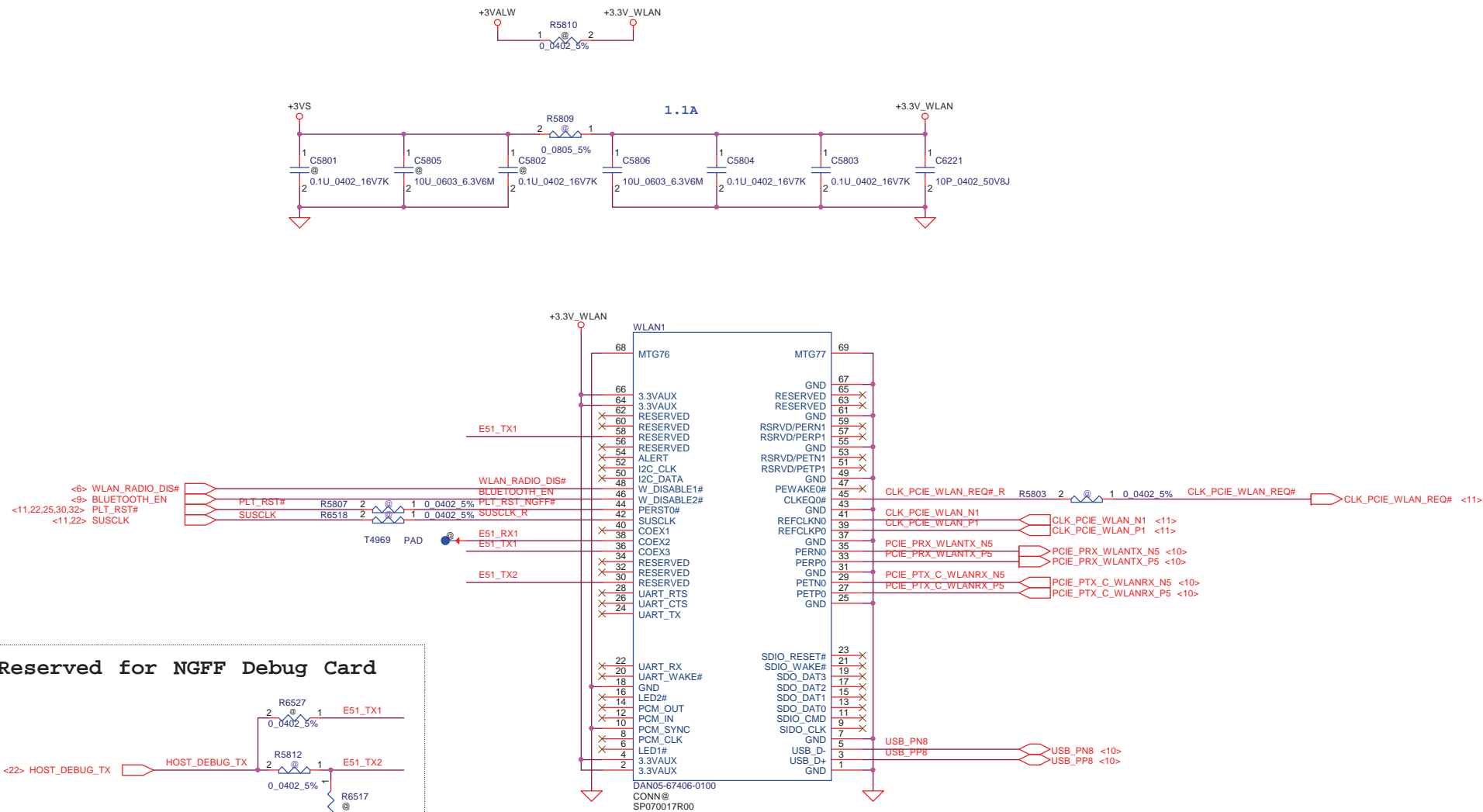


2/6 TX Cap change P/N,
Now It's 0402 0ohm resistor.

<10> SATA3_PRX_SSDTX_P2	SATA3_PRX_SSDTX_P2	CHD1	SSD@	1	2	0.01U_0402_16V7K	SATA3_PRX_C_SSDTX_P2
<10> SATA3_PRX_SSDTX_N2	SATA3_PRX_SSDTX_N2	CHD2	SSD@	1	2	0.01U_0402_16V7K	SATA3_PRX_C_SSDTX_N2
<10> SATA3_PTX_SSDRX_N2	SATA3_PTX_SSDRX_N2	CHD3	SSD@	1	2	0.01U_0402_16V7K	SATA3_PTX_C_SSDRX_N2
<10> SATA3_PTX_SSDRX_P2	SATA3_PTX_SSDRX_P2	CHD4	SSD@	1	2	0.01U_0402_16V7K	SATA3_PTX_C_SSDRX_P2

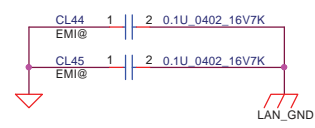
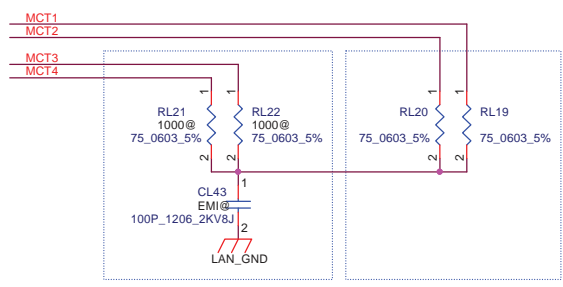
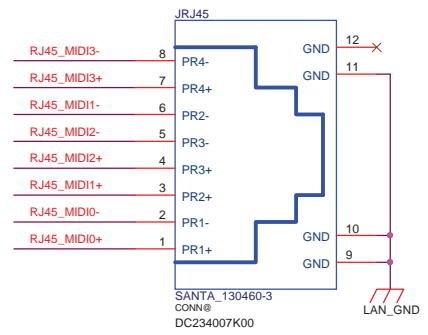
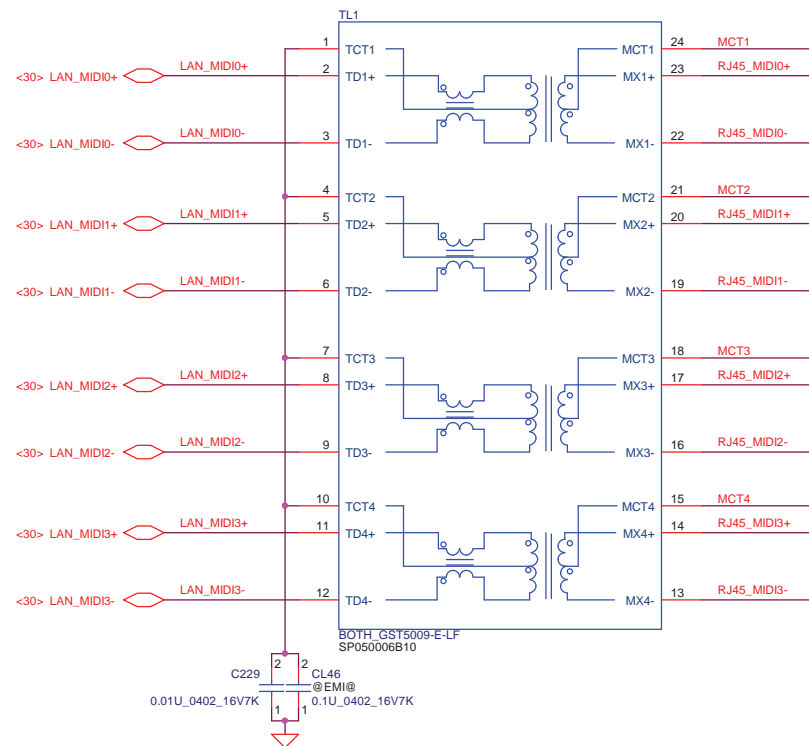


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Date:	Monday, June 08, 2016	Sheet	28	of	46	

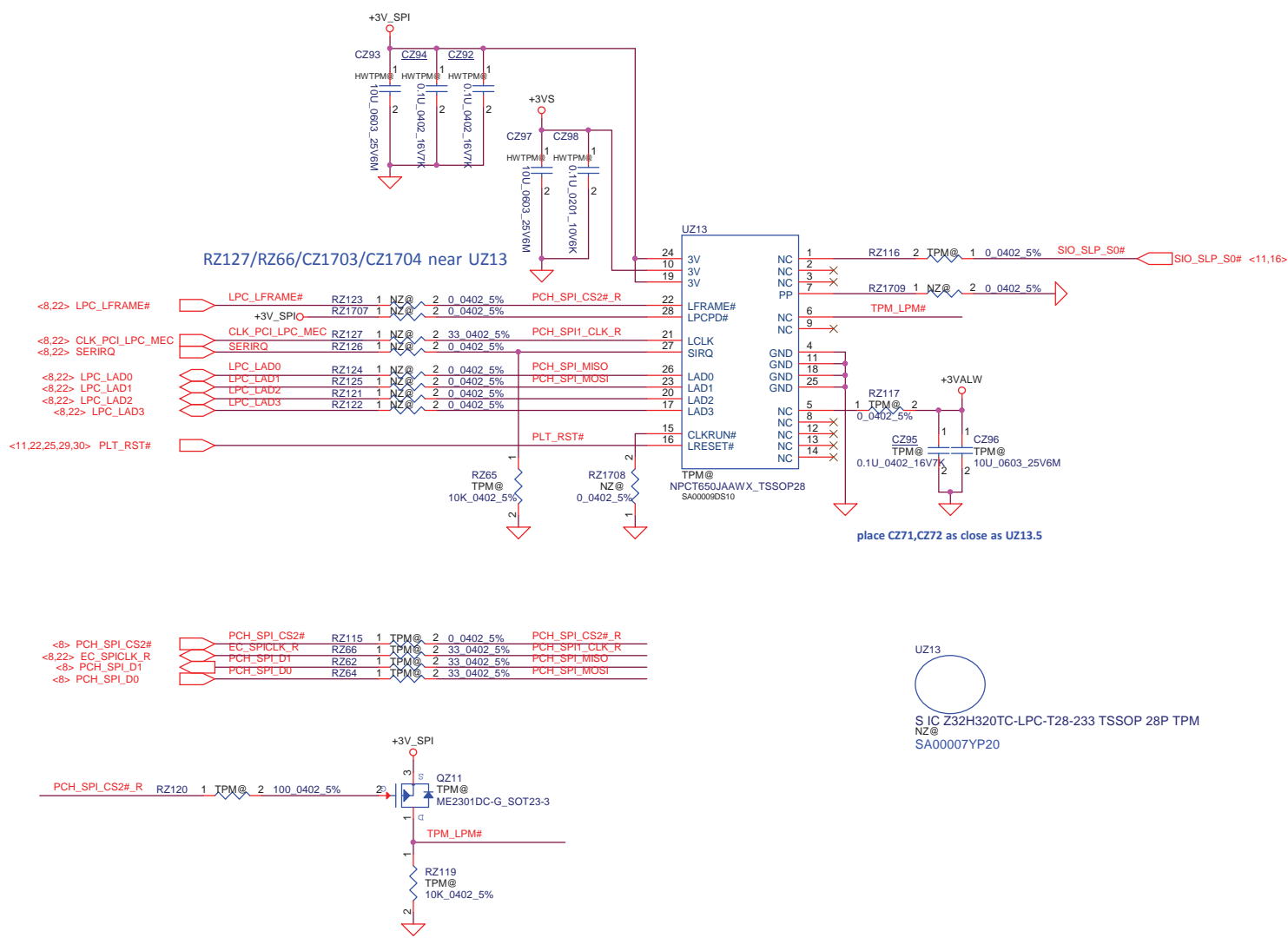


Support: Intel Dual Band Wireless-AC 3160

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				Size	Rev
				Document Number LA-D822P	
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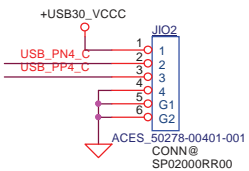
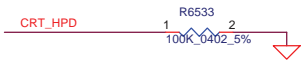
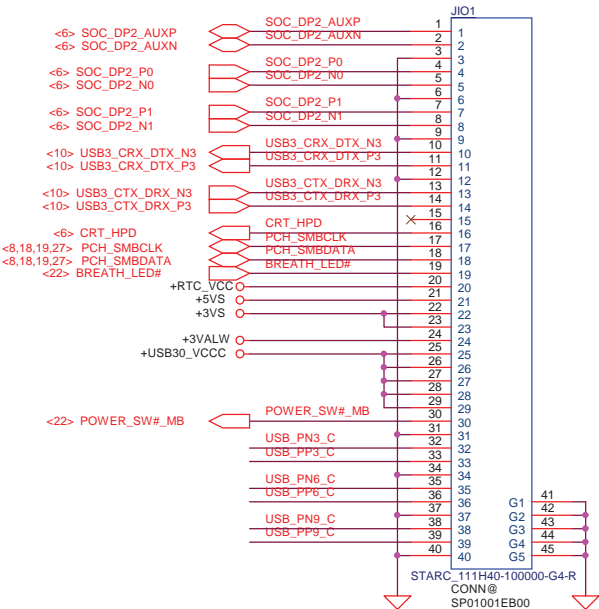
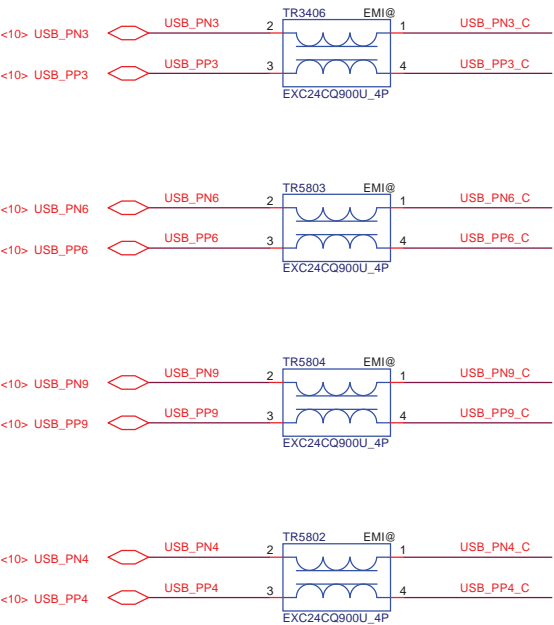


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Size	Custom	Document Number	LA-D822P	Rev	
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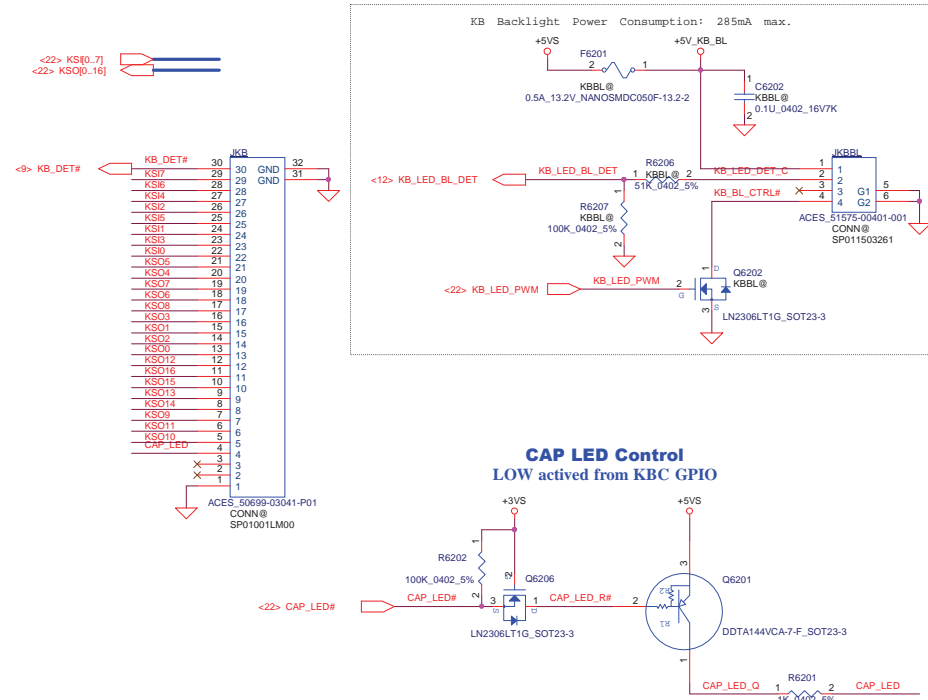
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I/O Board Connector

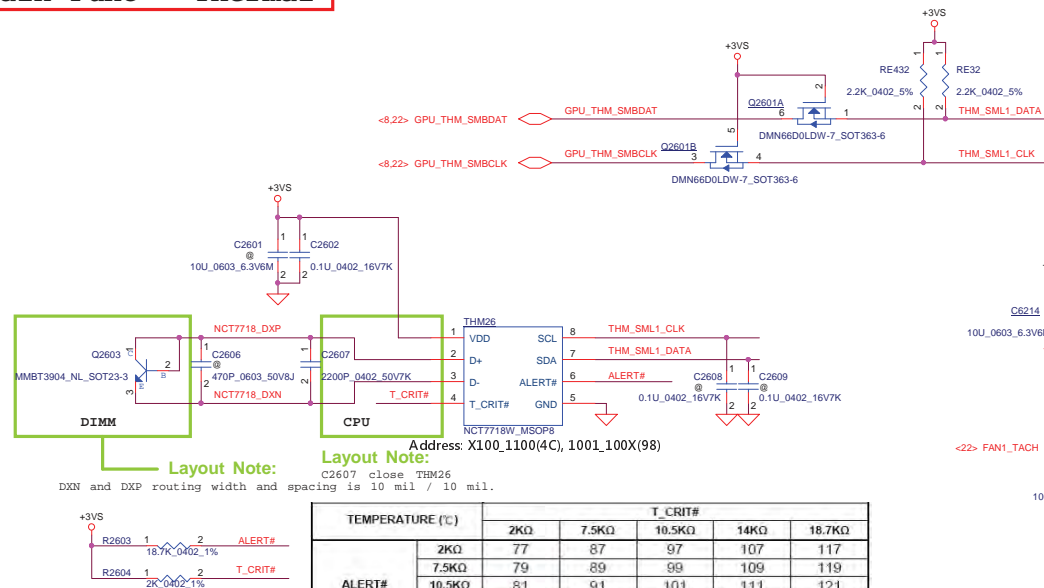


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Size		Document Number		Rev	
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LA-D822P		SP02000RR00		1.0	

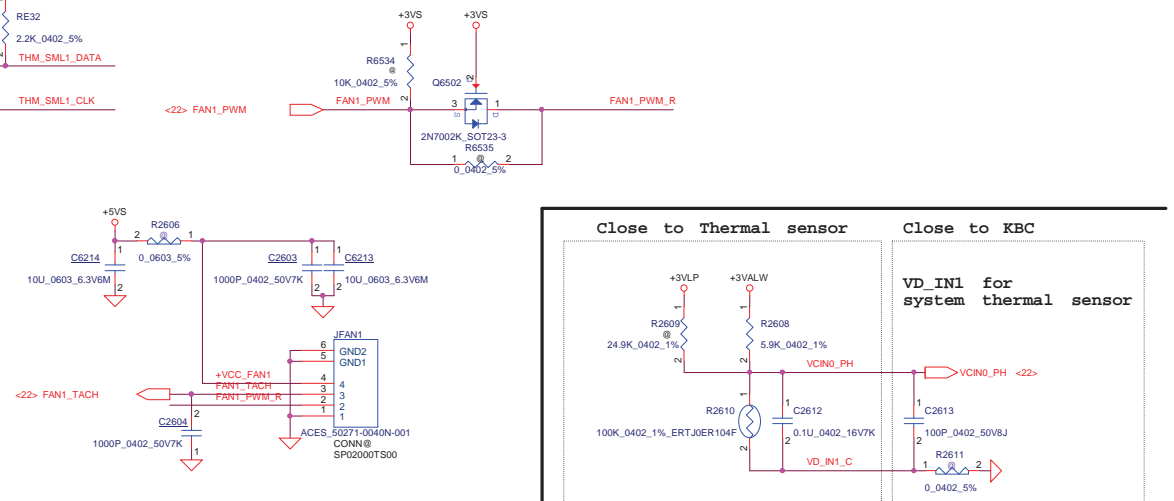
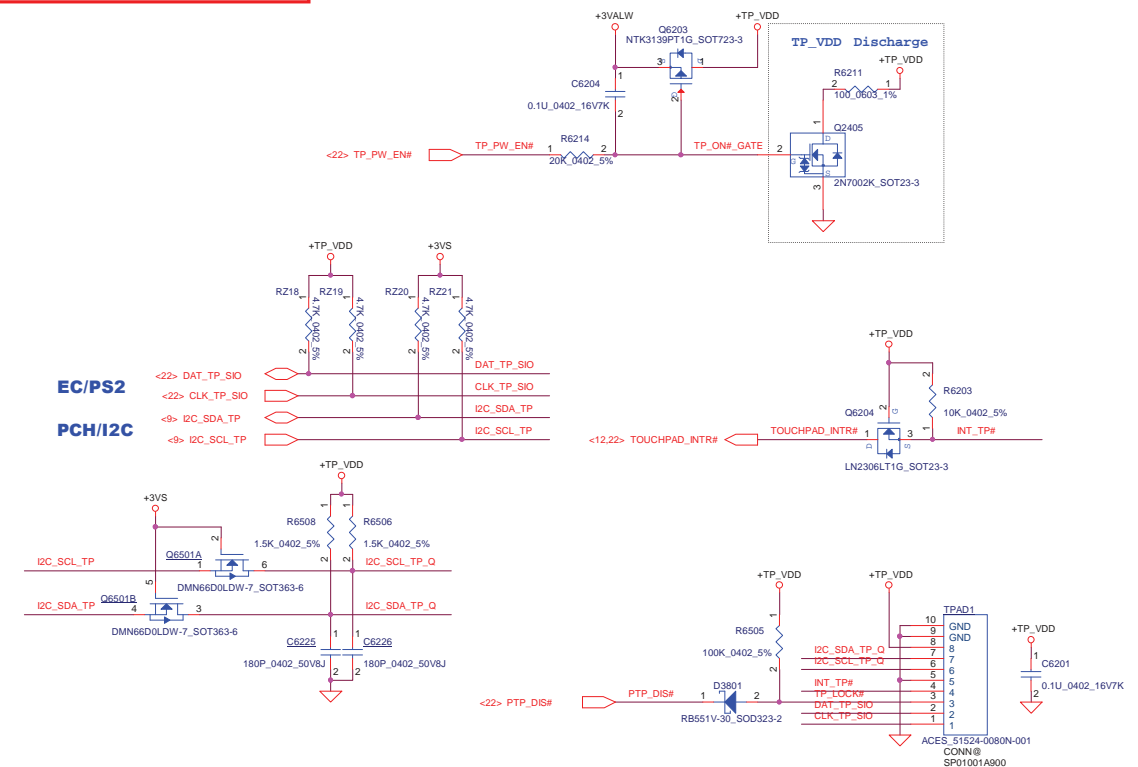
Keyboard Backlight (Reserved)



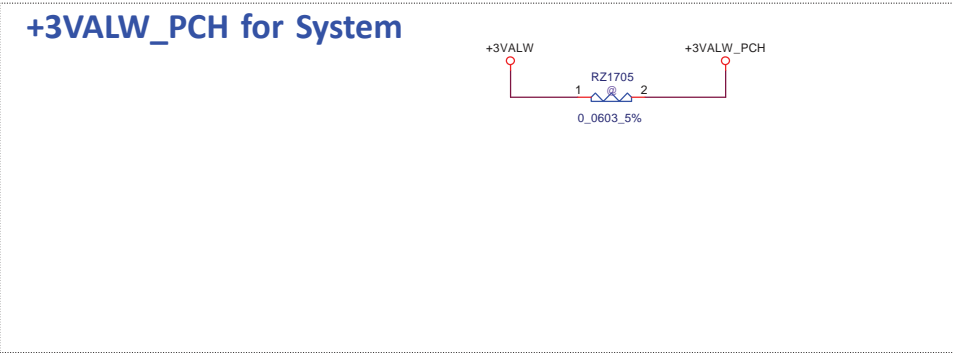
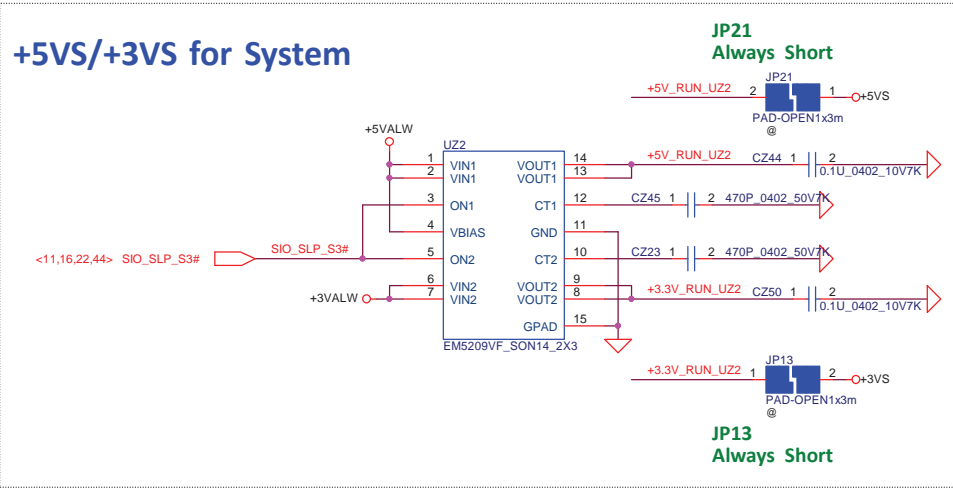
Main Func = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



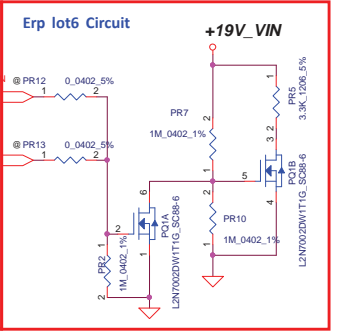
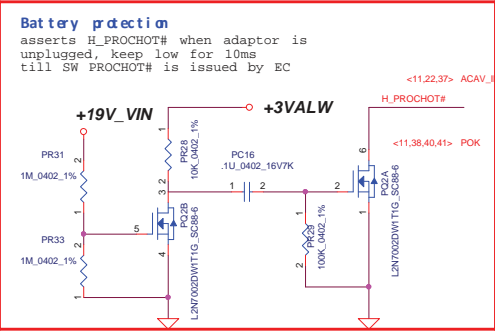
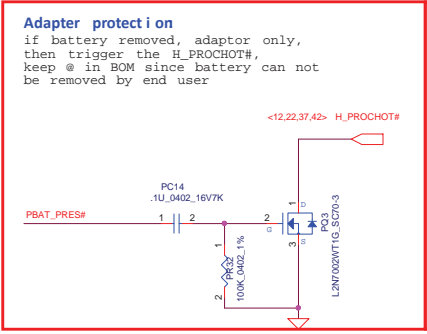
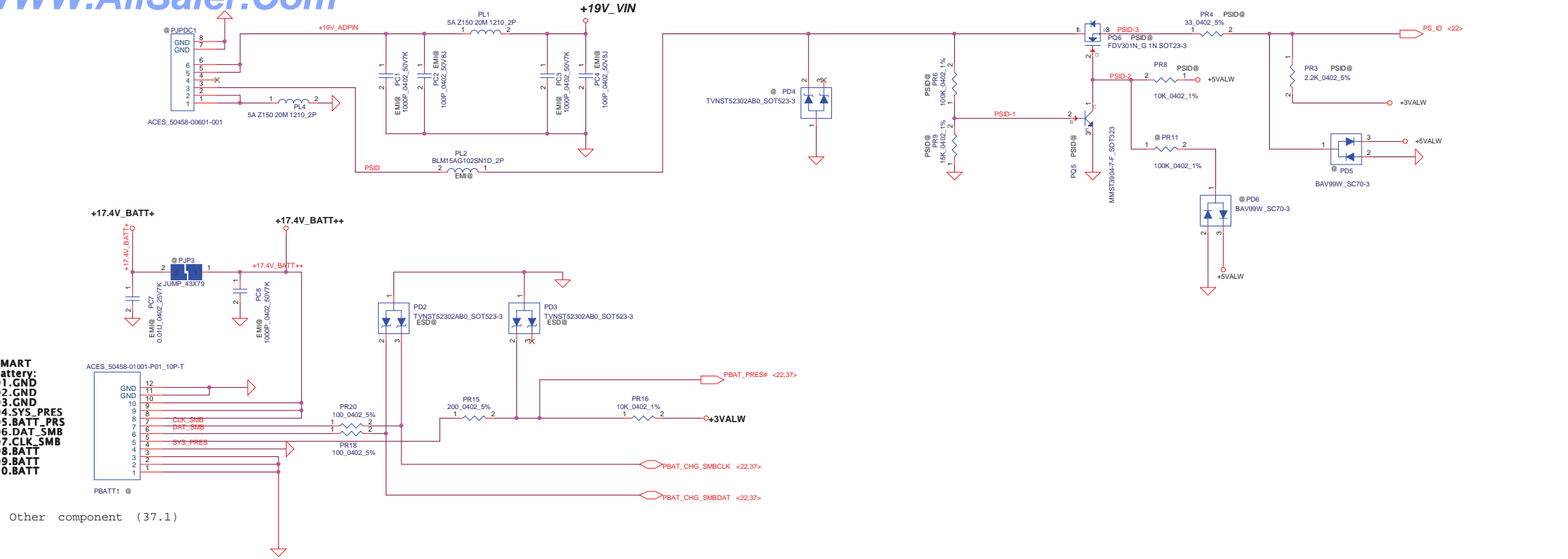
Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2015/07/09	Deciphered Date		2016/07/31	Title			
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						Size	Document Number		Rev
						LA-D822P		1.0	
Date: Monday, June 06, 2016						Sheet 34 of 46			



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Compal Electronics, Inc.			
Title		DC to DC	
Size	Document Number		Rev
	LA-D822P		1.0
Date:	Monday, June 06, 2016		Sheet 35 of 46

SMART
Battery:
01.GND
02.GND
03.GND
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT
09.BATT
10.BATT



15W_U22(SKI)
X63:PSID@/U22_SKI@/15W@_U22
X4P:EMIO/BSDO/RFO

15W_U22(KBL)
X63:PSID@/U22_KBL@/15W@_U22
X4P:EMIO/BSDO/RFO

28W_U23e
X63:PSID@/U23@/28W@
X4P:EMIO/BSDO/RFO

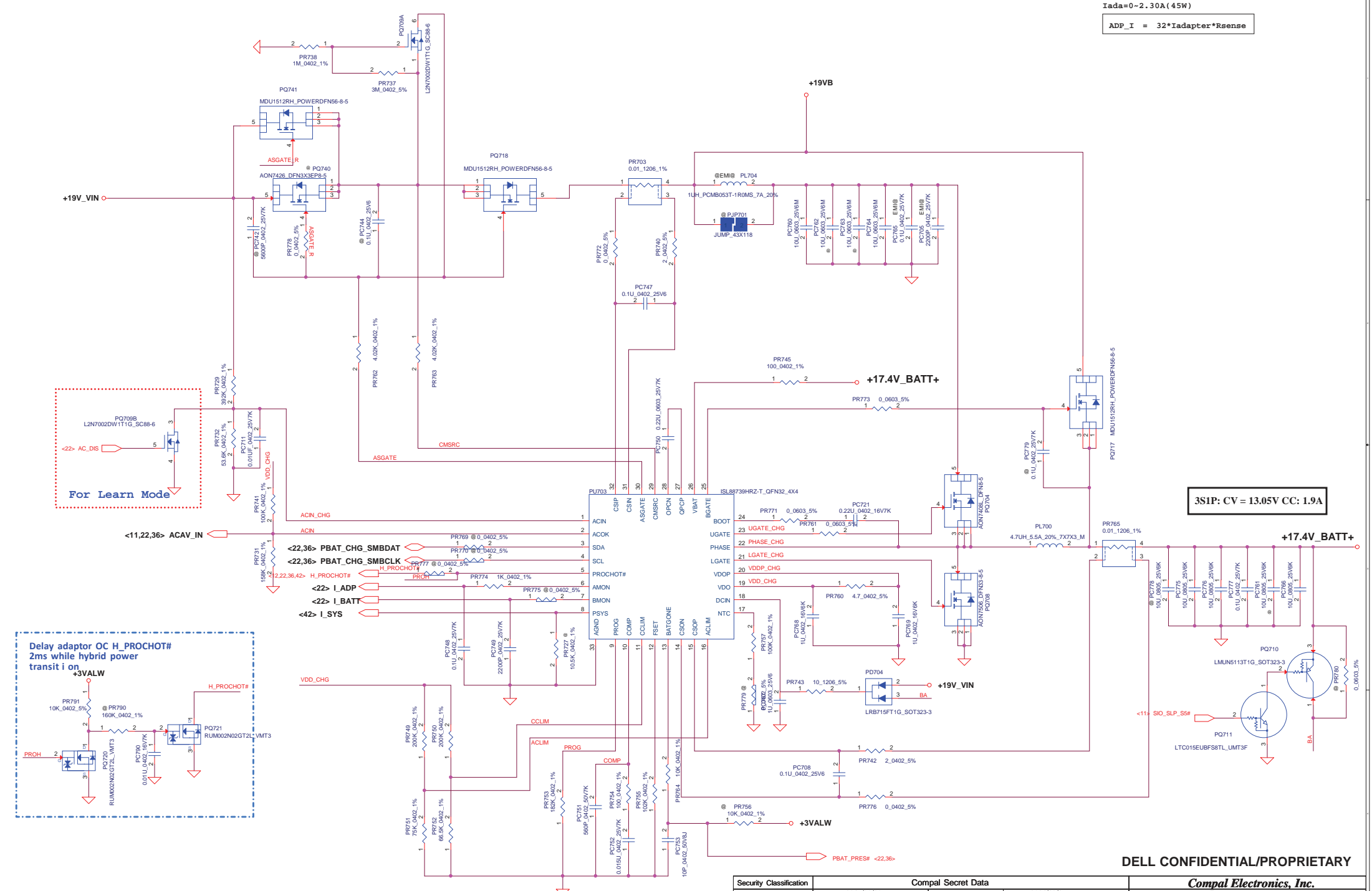
15W_U23e(Unused)
X63:PSID@/U23@/15W@_U22/15W@_U23
X4P:EMIO/BSDO/RFO

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Security Classification		Compal Secret Data		Title	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	PWR DCIN/BATT CONN/OTP	
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				Date:	Monday, June 05, 2016
				Sheet	36 of 46

Iada=0~3.33A (65W)
Iada=0~2.30A (45W)

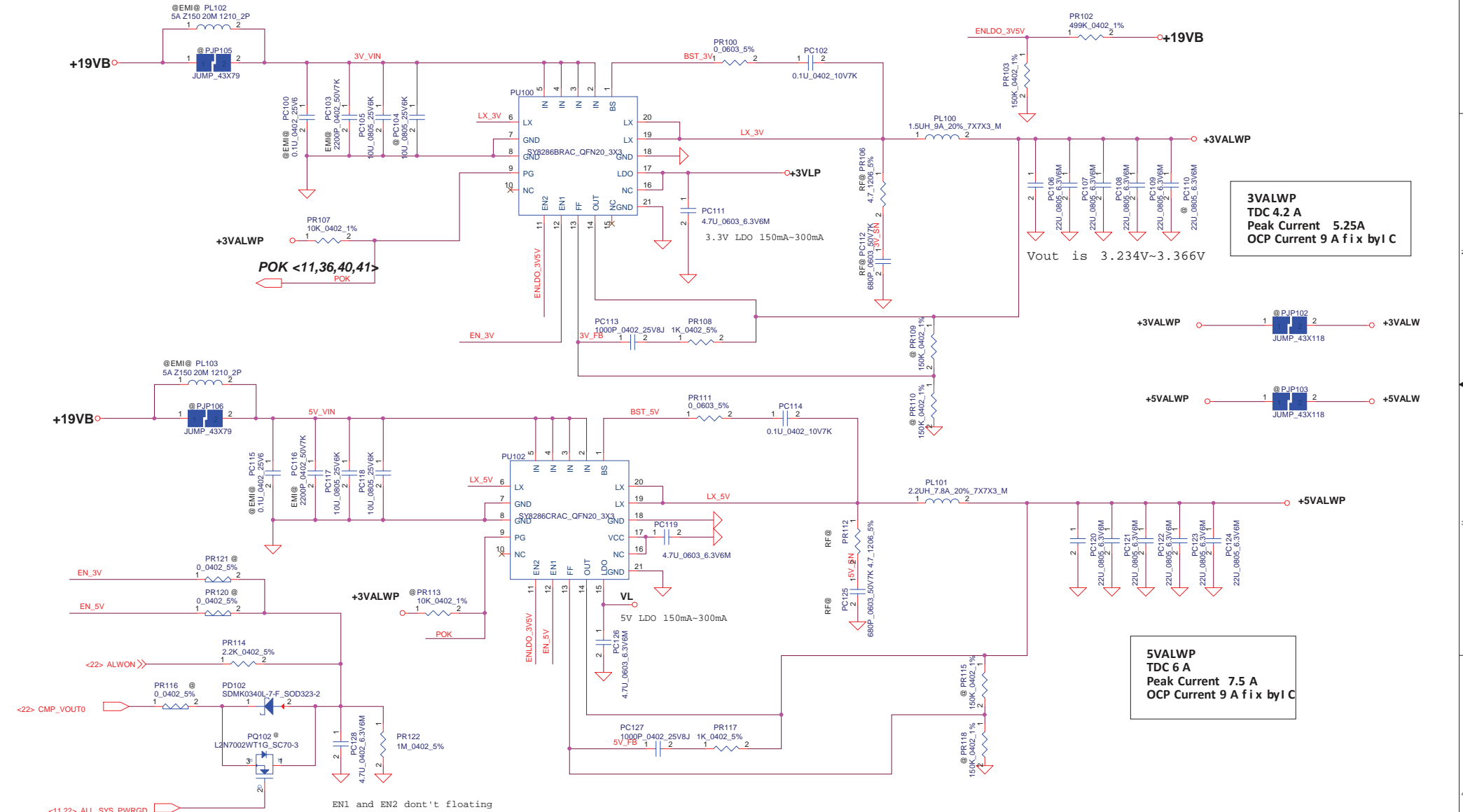
$ADP_I = 32 * I_{adapter} * R_{sense}$



3S1P: CV = 13.05V CC: 1.9A

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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title	
				PWR CHARGER	
				Size	Document Number
				Date	Monday, June 06, 2016
				Sheet	37 of 46



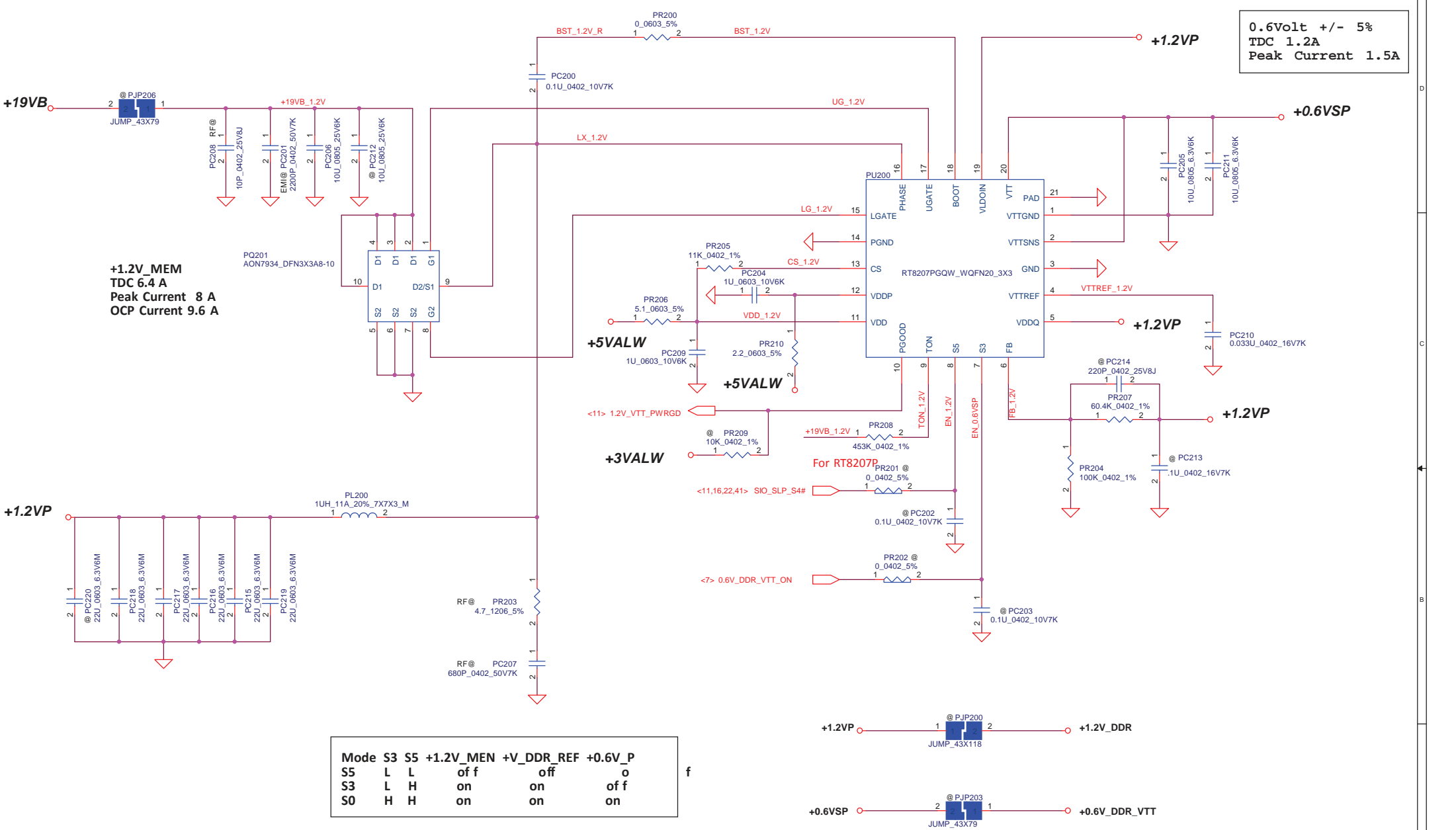
3VALWP
TDC 4.2 A
Peak Current 5.25A
OCP Current 9 A fix byl C

5VALWP
TDC 6 A
Peak Current 7.5 A
OCP Current 9 A fix byl C

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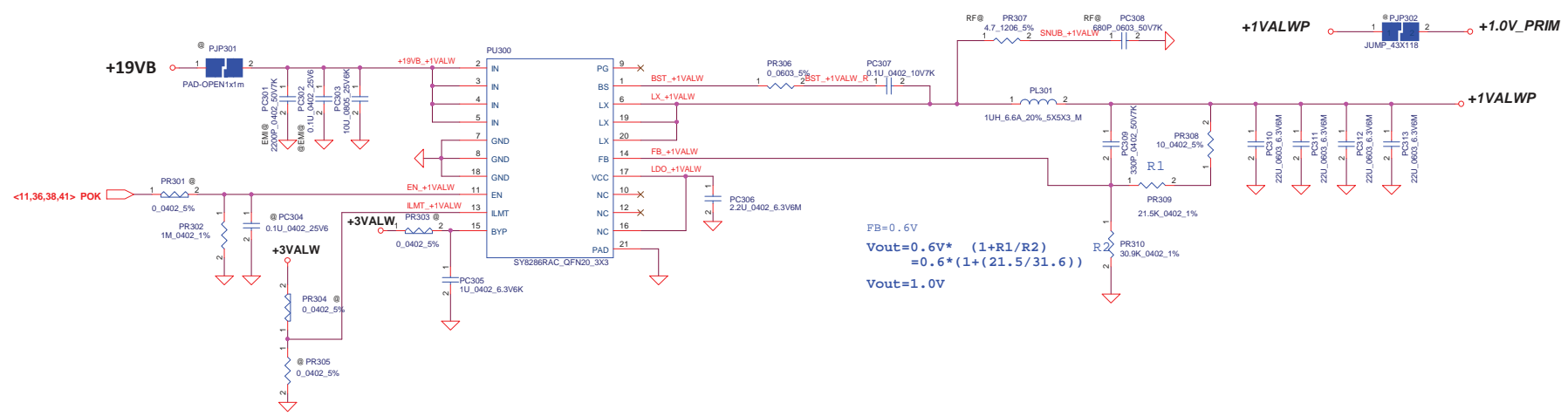
Compal Electronics, Inc.			
Title			
PWR_3.3VALWP/5VALWP			
Size	Document Number	Rev	
		X01(0.2)	
Date:	Monday, June 06, 2016	Sheet	38 of 46

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Security Classification		Compal Secret Data		Title	
Issued Date	2015/03/23	Deciphered Date	2014/12/15	PWR +1.2V_MEN/+0.6V_DDR_VTT	
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WWW.AliSaler.Com				Custom	Rev X01(0.2)
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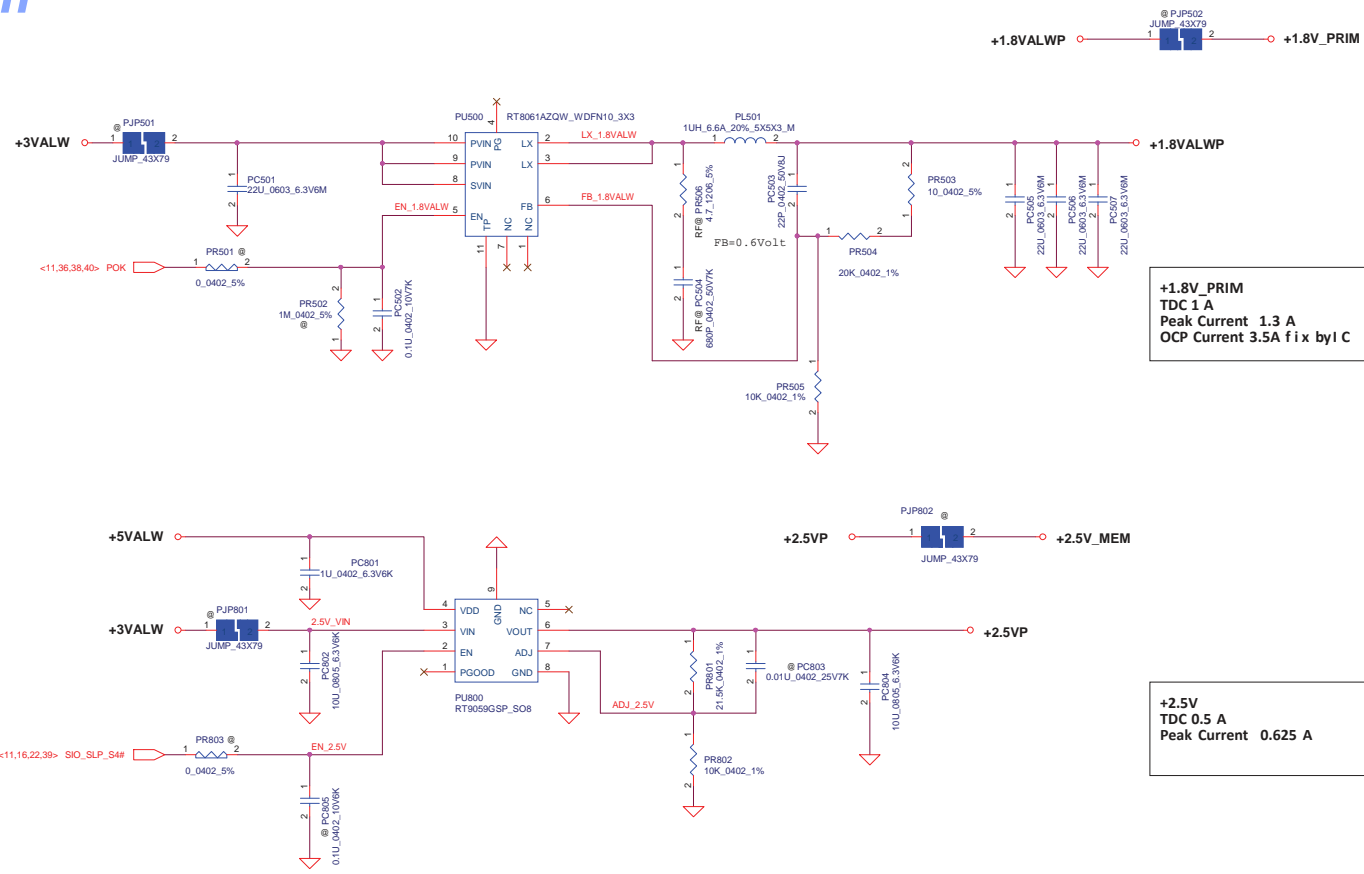
FB=0.6V
 $V_{out}=0.6V \cdot \left(1+\frac{R1}{R2}\right)$
 $=0.6 \cdot \left(1+\frac{21.5}{31.6}\right)$
 $V_{out}=1.0V$

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

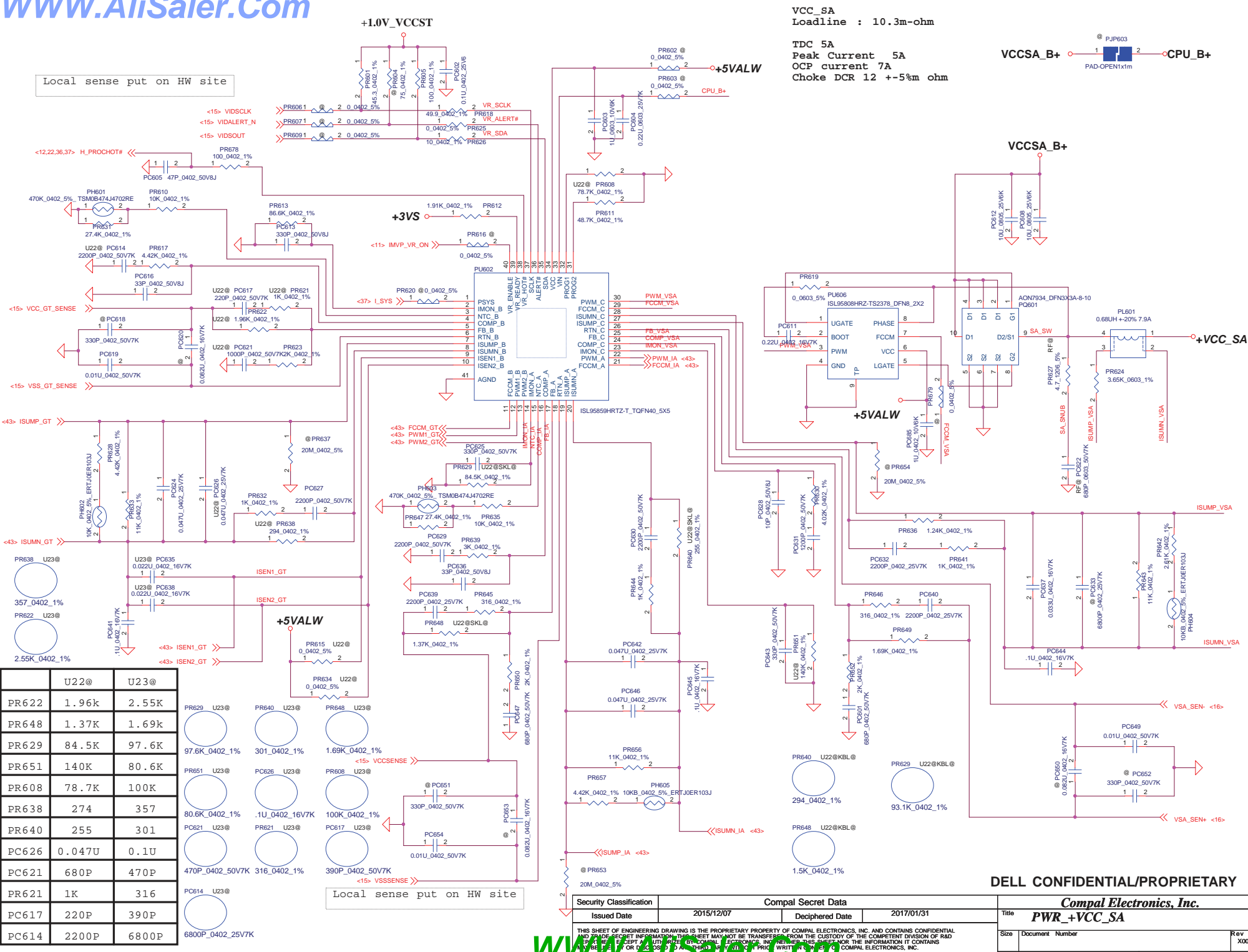
+1.0V_PRIM
TDC 6 A
Peak Current 8.6 A
OCP Current 12 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

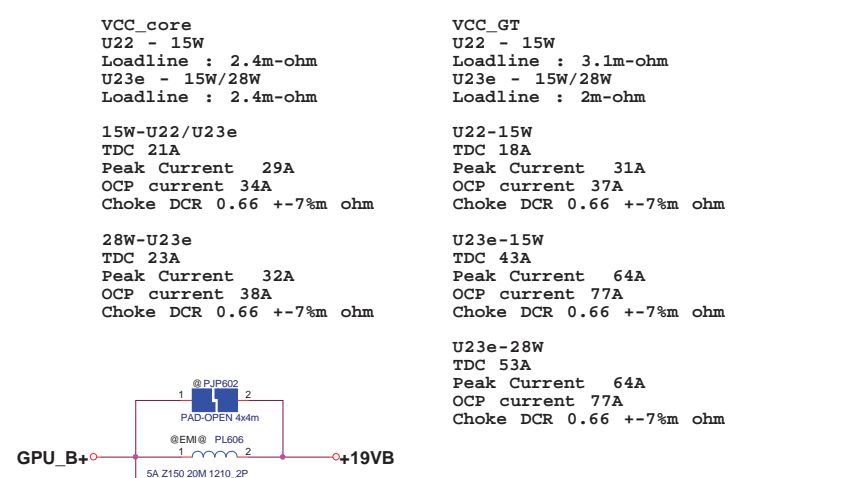
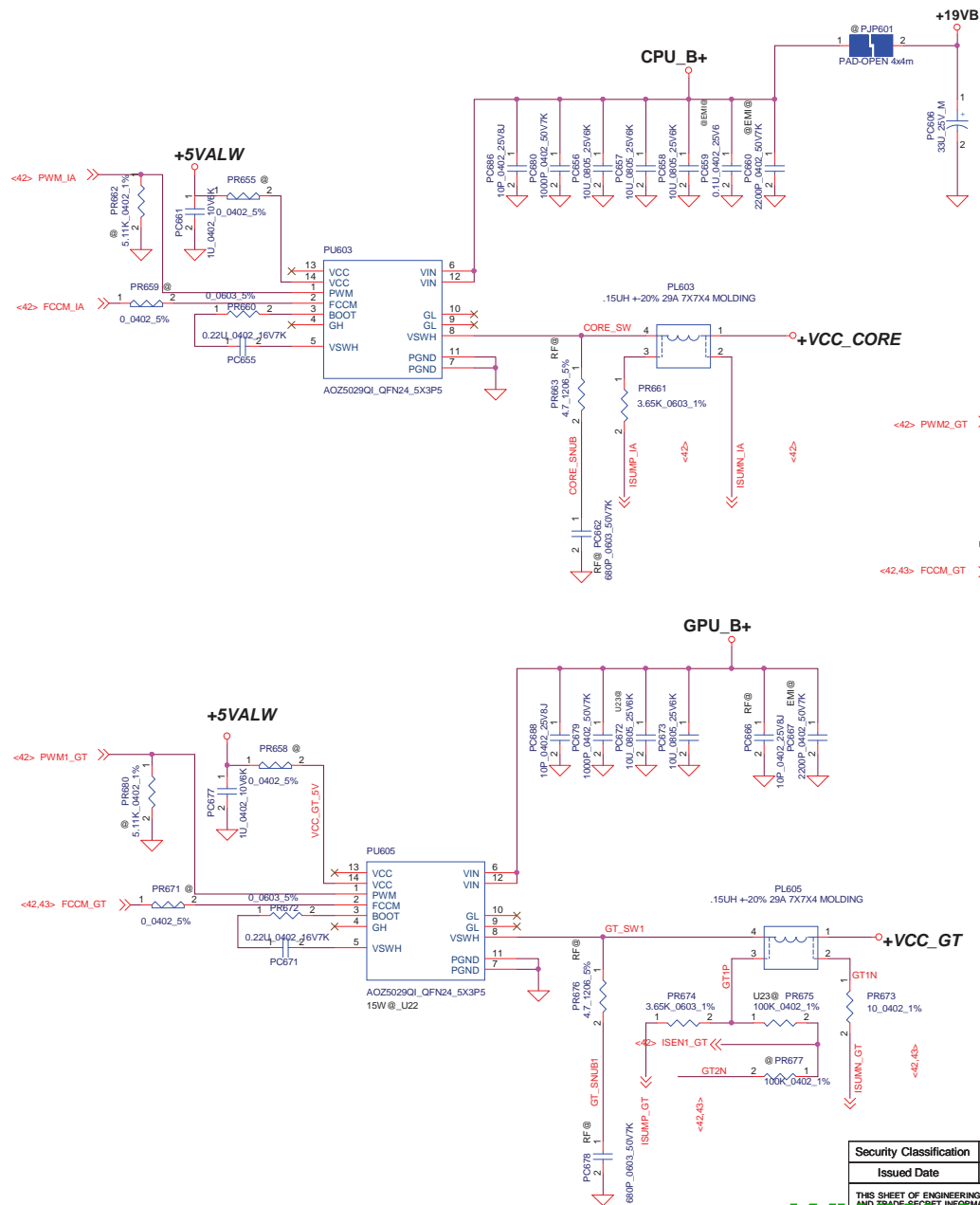
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Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title
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Size	C	Document Number		Rev
Date:	Monday, June 06, 2016	Sheet	41 of 46	X01(0.2)





VCC_core
U22 - 15W
Loadline : 2.4m-ohm
U23e - 15W/28W
Loadline : 2.4m-ohm

15W-U22/U23e
TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7% ohm

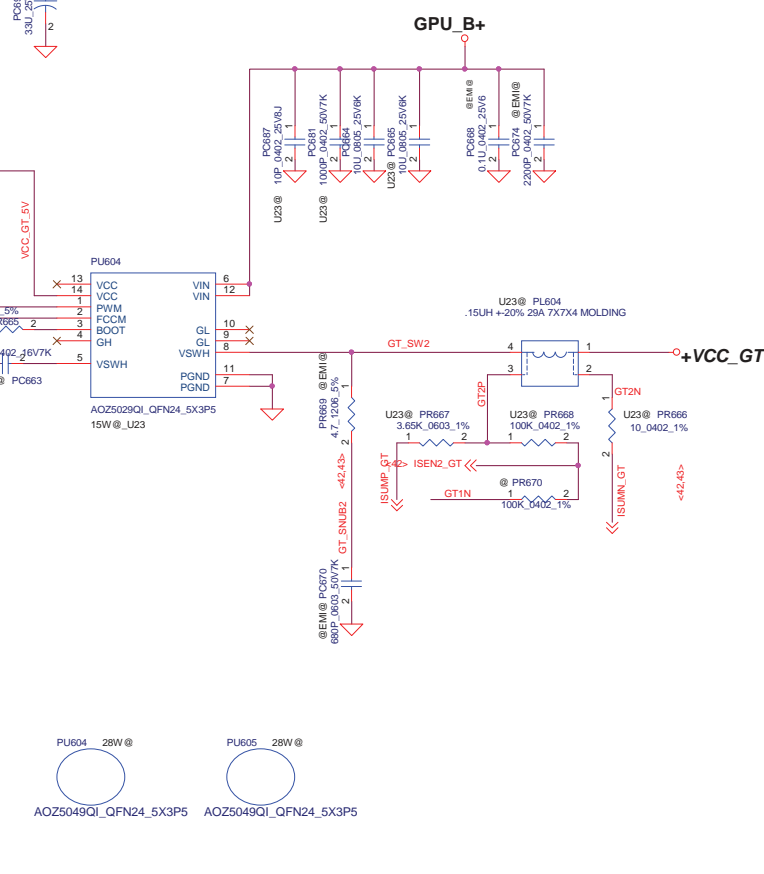
28W-U23e
TDC 23A
Peak Current 32A
OCP current 38A
Choke DCR 0.66 +-7% ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W/28W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7% ohm

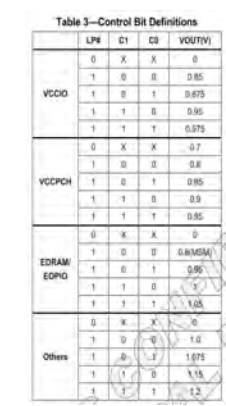
U23e-15W
TDC 43A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7% ohm


U23e-28W
TDC 53A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7% ohm



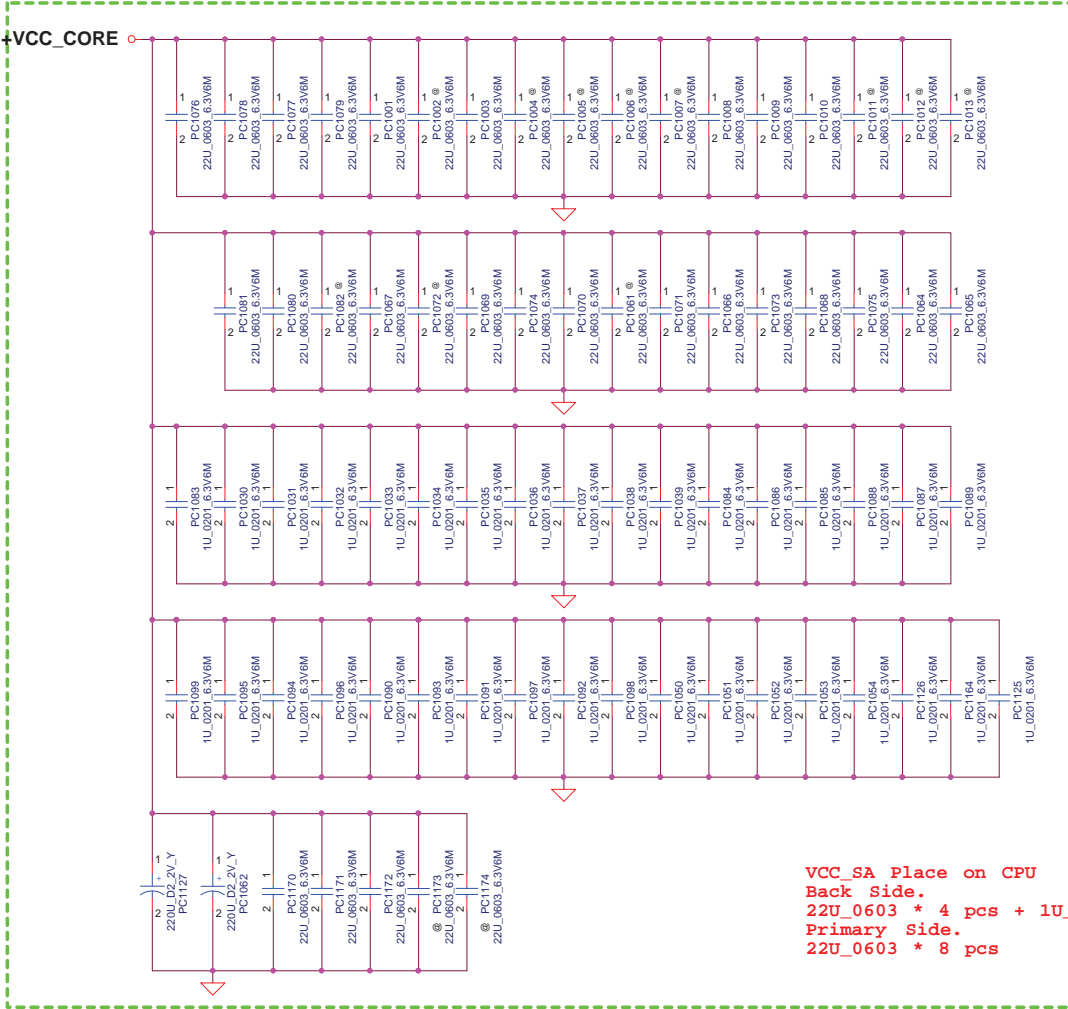
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2015/12/07		2017/01/31		PWR +VCC_core and +VCC_GT	
2015/12/07		2017/01/31		Size Document Number	
2015/12/07		2017/01/31		Rev X00	
2015/12/07		2017/01/31		Date: Monday, June 06, 2016	
2015/12/07		2017/01/31		Sheet 43 of 46	

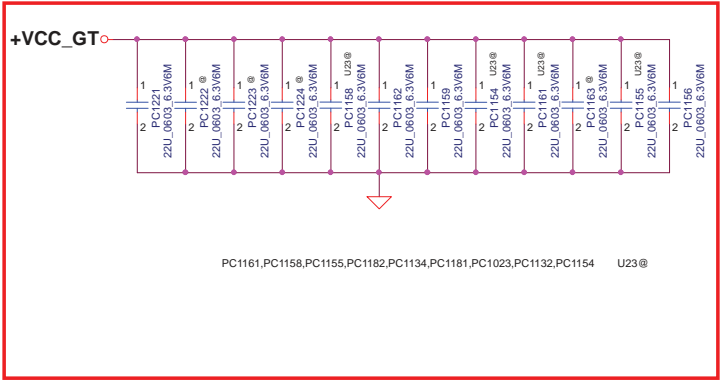


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Issued Date		2015/12/07	Deciphered Date		2017/07/31
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				Size	
				Rev	X00
Date: Monday, June 06, 2016				Sheet	44 of 46

VCC_CORE Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*35 pcs
Primary Side.
22U_0603 * 20 pcs+220u_D2*2 pcs



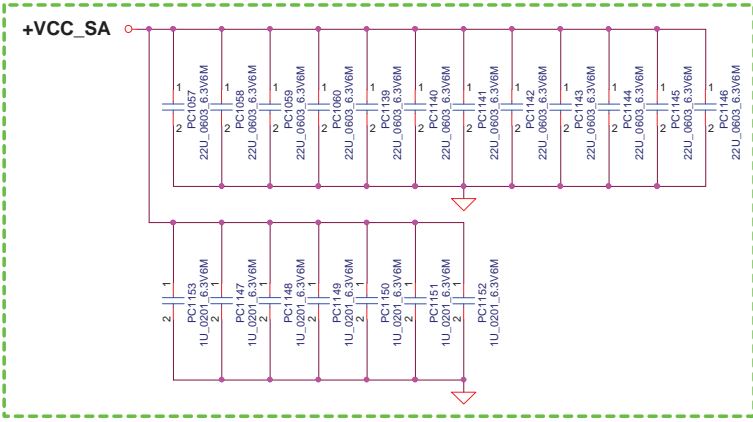
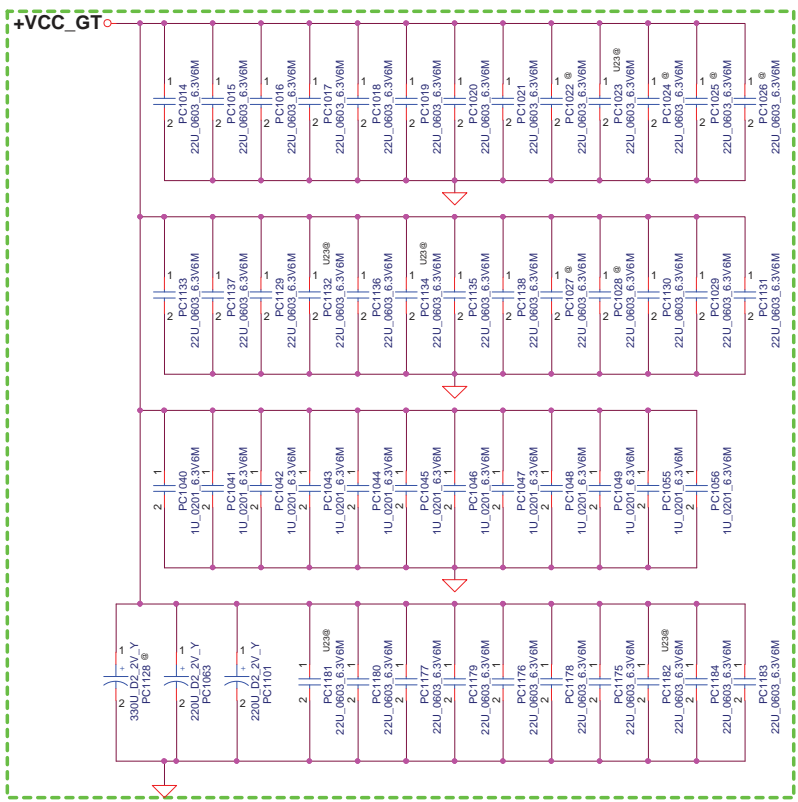
VCC_SA Place on CPU
Back Side.
22U_0603 * 4 pcs + 1U_0201*7 pcs
Primary Side.
22U_0603 * 8 pcs



PC1161,PC1158,PC1155,PC1182,PC1134,PC1181,PC1023,PC1132,PC1154 U23@

For GTX

VCC_GT Place on CPU
Back Side.
22U_0603 * 13 pcs +1U_0201*12 pcs
Primary Side.
22U_0603 * 13 pcs +220u_D2*2 pcs



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Security Classification				Compal Secret Data		Title	
Issued Date	2014/11/05	Deciphered Date	2014/12/15	Compal Electronics, Inc.		PWR CPU&VGA bulk and MLCC	
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P37	PWR	20160303	COMPAL	to change charger IC	change charger IC(PU703) to ISL88739	0.2(x01)
2	P39 P43 P45 P46	PWR	20160303	COMPAL	to prevent RF issue	add PC208 add PC666,PR676,PC678 add PC1116,PR1122,PC1109, add PC1402,PR1408,PC1408	
3	P42	PWR	20160303	COMPAL	to adjust +VCC_CORE and +VCC_GT load line	change PR622 to 1.91K,PR638 to 287 ohm,PC626 to 0.1uF,PC642 to 0.1uF	
4	P36,P42	PWR	20160303	COMPAL	to save layout space	delete PL3,PL602(reserve location)	
5	P36	PWR	20160303	COMPAL	to fix battery connector ME issue	to change battery connector	
6	P37	PWR	20160304	COMPAL	to fix Temp/Voltage 19.5V DC-IN issue	change PR732 to 53.6K	
7	P44	PWR	20160304	COMPAL	to fix DFB solder open problem	change PC1127,PC1062,PC1128 footprint	
8	P38	PWR	20160308	COMPAL	to prevent OTP functions abnormal issue	to reserve PQ102 and connect to ALL_SYS_PWRGD	
9	P37	PWR	20160316	COMPAL	to save layout space by EMI request	change PC760,PC762,PC763,PC764 to 0603 size and delete PR766,PC767	
10	P43	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's load line	to unmount PC624 and PC646	
11	P45	PWR	20160328	COMPAL	according to test result to adjust VCC_CORE and GT_CORE's output MLCC's location(only change BOM) and bulk cap	unmount:PC1021,PC1135,PC1133,PC1131,PC1022,PC1025,PC1027, PC1028,PC1063, PC1008,PC1003,PC1011,PC1072,PC1076,PC1071,PC1081,PC1082,PC1004, PC1007,PC1012 to mount:PC1176,PC1175,PC1177,PC1179,PC1178,PC1180,PC1183,PC1184, PC1170,PC1173,PC1174 to change PC1127,PC1062 to 220uF/9m ohm	
12	P36	PWR	20160429	COMPAL	To improve EMI and reduce inrush current to mount n filter' s bead and change cap	unmount:PL1,PL4 change:PC2,PC4 to 100pF	
13	P37	PWR	20160429	COMPAL	ISL88739 doesn't support PSYS function	unmount:PR727 change PR774 to 1K ohm change PC748 0.1uF	0.3(x02)
14	P39	PWR	20160429	COMPAL	to adjust 1.2V OCP to 10.2A	change PR205 to 11K	
15	P37	PWR	20160429	COMPAL	to aviod inrush to damage MOS	to reserve PQ741	

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Issued Date	2015/07/15	Deciphered Date	2016/07/31	Title		
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						1.0(00)
				Date:	Monday, June 06, 2016	Sheet 46 of 46